STUDY AND ANALYSIS OF NOT & NAND GATE USING VARIOUS LOW POWER TECHNIQUES

Kapil Mangla, Prof. (Dr.) Anil Kumar

Al-falah School of Engineering & Technology Faridabad, Haryana

kapilmangla005@gmail.com, anil4k@gmail.com

Abstract-

Designing high-speed low-power circuits with CMOS technology has been a major research problem for many years. The increasing demand for low-power design can be addressed at different design levels, such as software, architectural, algorithmic, circuit, and process technology level. This paper presents different approaches to reduce power consumption of any arbitrary combinational logic circuit by applying power minimization techniques at circuit level. First find out the low power on different width & length ratio. And result of best width and length ratio used in different power consumption techniques. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level. Conventional NAND gate and NOT gate are designed and then compared with the stack NAND and stack NOT and adiabatic NAND and Adiabatic NOT using 180nm technology.

***Keywords*:** CMOS Circuit, VLSI, Combinational Circuits, Tanner EDA, Power.

I. INTRODUCTION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems.

Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability.

It is more convenient to talk about power dissipation of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI)

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this Work, power consumption depend upon the width and length ratio is presented. If we change the width and length of the device then it's current and gate capacitance changes. In this work i have used the 180nm technology. So that the length is fixed but change in the width. So the result is depending upon the different width and length ratio. Current will increase if the width of transistor increases and gate capacitance also increase if the width of transistor increase and vice versa. The power consumption is also depending upon the current in the circuit and current is depending upon the width and length ration.

II. OVERVIEW OF POWER DISSIPATION

As we all know that CMOS work in three regions. Cut-off region, saturated region and non saturated regions. So the current is different in different regions.

In cut-off region :

$$I_{ds} = 0 \; for \; V_{gs} < V_{th}$$

In linear / non-saturated / active region:

$$I_{ds} = \frac{KW}{L}\left[(V_{gs} - V_{th})^2 - \frac{V_{ds}}{2}\right] V_{ds}$$

In Saturation Region:

$$I_{ds} = \frac{KW}{2L}(V_{gs} - V_{th})^2$$

Static CMOS gates are very Power Efficient because they dissipate nearly ZERO power while operating in static state. Power was the secondary consideration behind speed and area. As transistor counts and clock frequencies have increased, power consumption has skyrocketed and now is a primary design constraint.

The instantaneous power P(t) drawn from the power supply is proportional to the supply current iDD(t) and the supply voltage VDD.

$$Instantaneous\ Power: \quad P(t) = i_{DD}(t).V_{DD}$$

$$Energy\ Consumed: \quad E = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

$$Average\ Power: \quad \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

III. STACKING TECHNIQUE FOR POWER REDUCTION

One technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors. Fig. 1 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub-threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

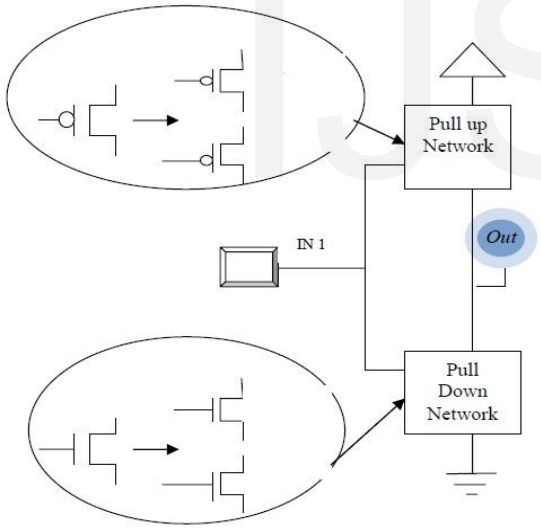


FIG. 1 CMOS CIRCUIT USING STACKING APPROACH

IV. ADIABATIC TECHNIQUE FOR POWER REDUCTION

The word ADIABATIC comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS.

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

Adiabatic switching principle is one of the best Power reduction techniques having many advantages over other techniques like simple to design, no complexity increases, and great reduction in power dissipation.

Basically adiabatic switching principle states that during the transition from logic 0 to logic 1 we need the power supply but transition from logic 1 to logic 0. We don't need the power supply. If at that time we make the power supply off we can save the power dissipation because power dissipation is directly proportional to the supply voltage.

This can be done by changing the voltage source either by sinusoidal voltage source or by Pulse and adjust the supply voltage in such a way that during the transition from logic 1 to logic 0 the supply voltage comes into off state and in this way the power dissipation is reduced up to much extent because as told earlier the power dissipation is directly proportional to supply voltage.

V. PROPOSED WORK

Logic gates are fundamental building blocks of digital integrated circuits . Logic gate is idealized or physical device implementing a Boolean function i.e., it performs a logical operation on one or more inputs and produces a single logical output. There are seven basic logic gates: NOT, AND, OR, NAND, NOR, XOR, XNOR. In this paper we will be implementing on NOT Gate / Inverter & NAND Gate.

A. NOT Gate / Inverter

Operation When V_{in} is high and equal to V_{DD}; the NMOS transistor is on, while the PMOS is off. A direct path exists between V_{out} and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS transistor is off and PMOS transistor is on. A path exists between V_{DD} and V_{out}, yielding a high output voltage. The gate clearly functions as an inverter.

Designing for Different W/L Ratio

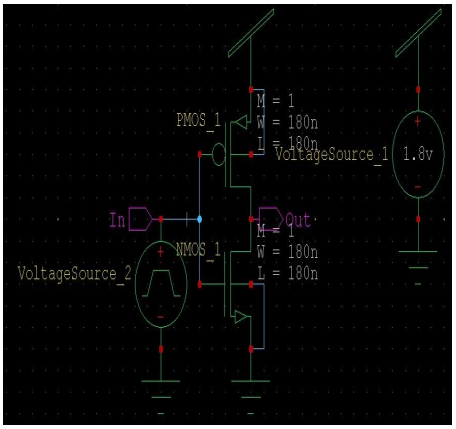


Fig.2 1:1 Ratio CMOS Inverter

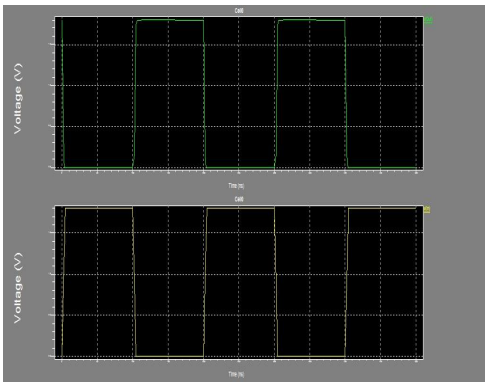


Fig.3 Waveform for Voltage of 1:1 Ratio CMOS Inverter

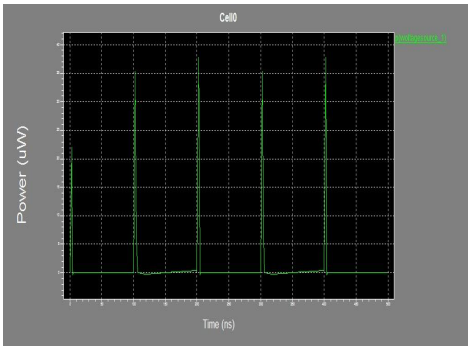


Fig.4 Waveform for Power of 1:1 Ratio CMOS Inverter

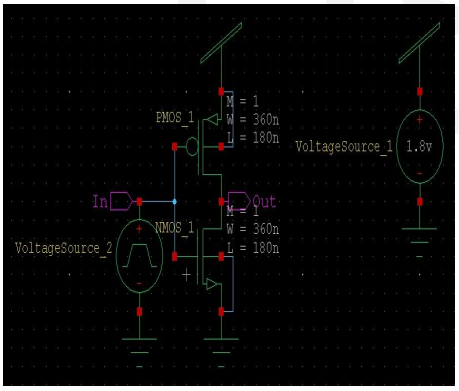


Fig.5 2:1 Ratio CMOS Inverter

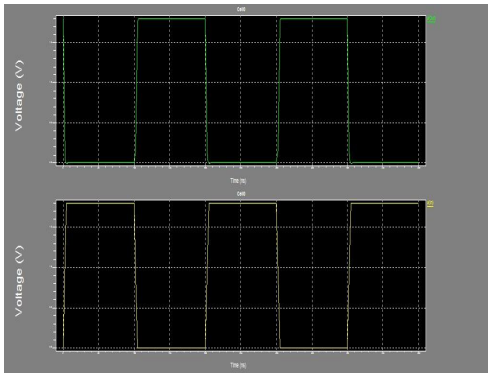


Fig.6 Waveform for Voltage of 2:1 Ratio CMOS Inverter

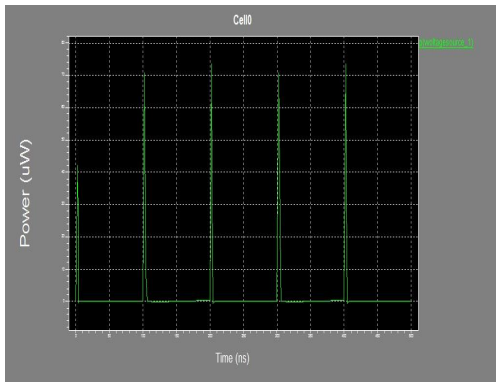


Fig.7 Waveform for Power of 2:1 Ratio CMOS Inverter

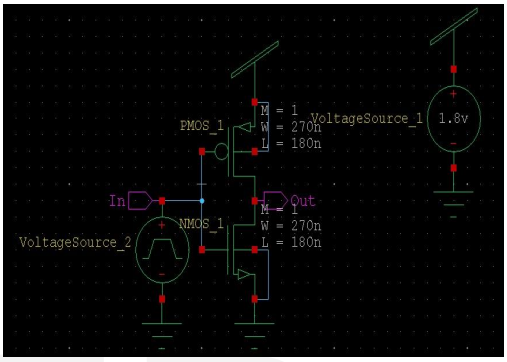


Fig.8 3:2 Ratio CMOS Inverter

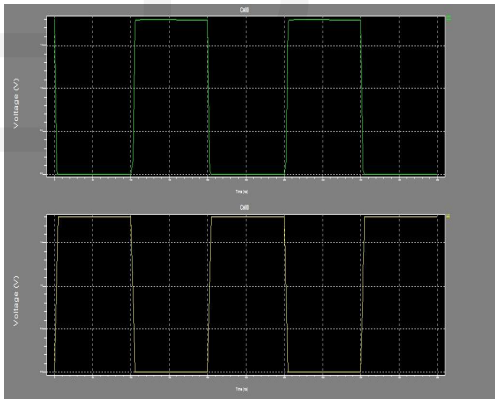


Fig.9 Waveform for Voltage of 3:2 Ratio CMOS Inverter

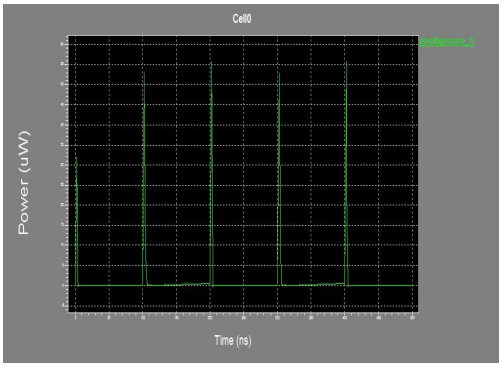
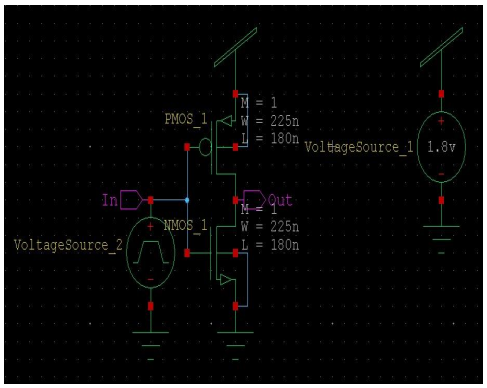


Fig.10 Waveform for Power of 3:2 Ratio CMOS Inverter



Fif.11 5:4 Ratio CMOS Inverter

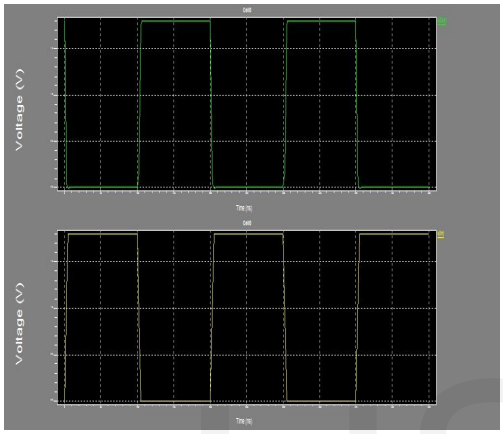


Fig.12 Waveform for Voltage of 5:4 Ratio CMOS Inverter

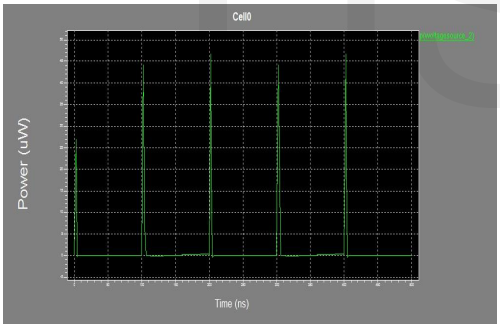


Fig.13 Waveform for Power of 5:4 Ratio CMOS Inverter

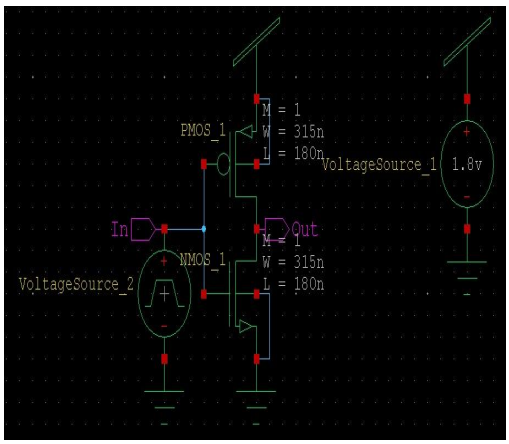


Fig.14 7:4 Ratio CMOS Inverter

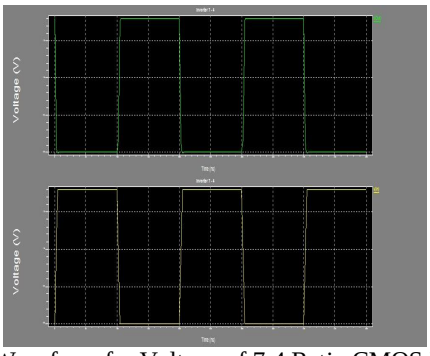


Fig.15 Waveform for Voltage of 7:4 Ratio CMOS Inverter

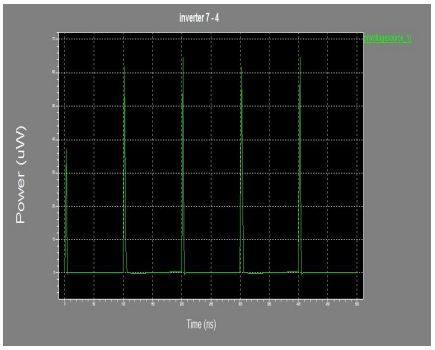


Fig.16 Waveform for Power of 7:4 Ratio CMOS Inverter

Conventional

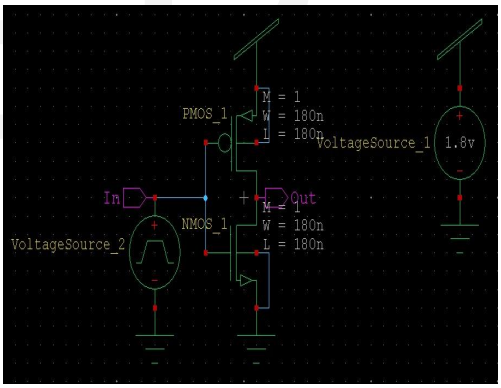


Fig.17 Conventional CMOS Inverter

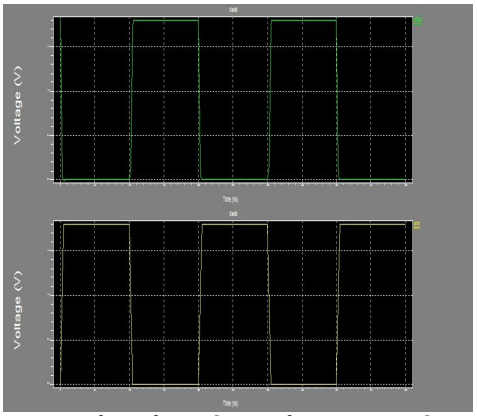


Fig.18 Waveform for Voltage of Conventional CMOS Inverter

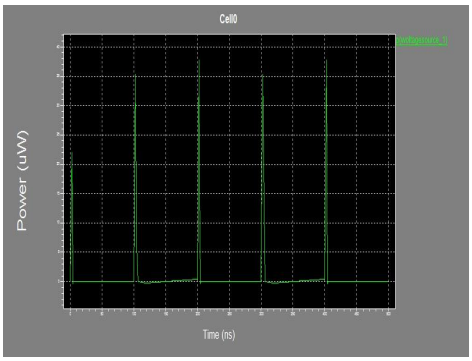


Fig.19 Waveform for Power of Conventional CMOS Inverter

Stacking

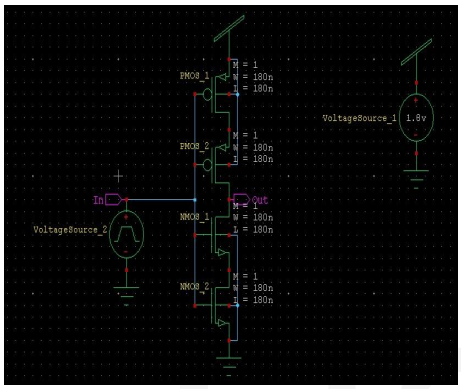


Fig.20 Stacking CMOS Inverter

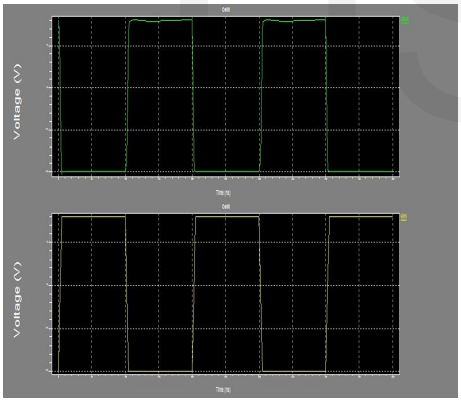


Fig.21 Waveform for Voltage of Stacking CMOS Inverter

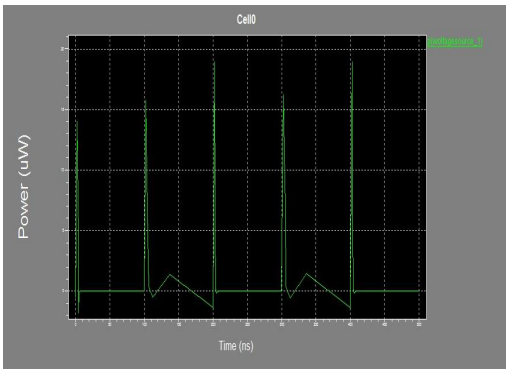


Fig.22 Waveform for Power of Stacking CMOS Inverter

Adiabatic

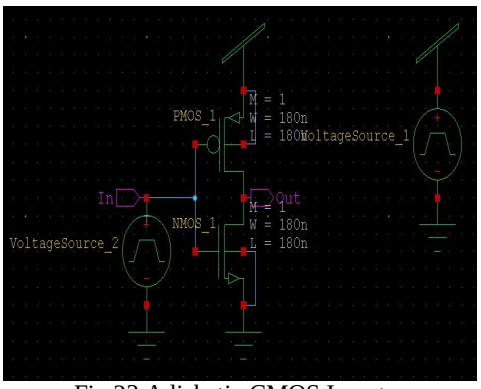


Fig.23 Adiabatic CMOS Inverter

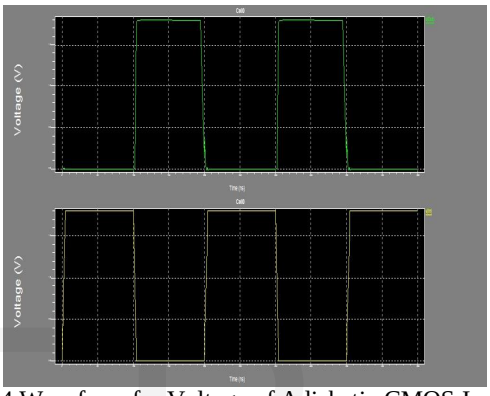


Fig.24 Waveform for Voltage of Adiabatic CMOS Inverter

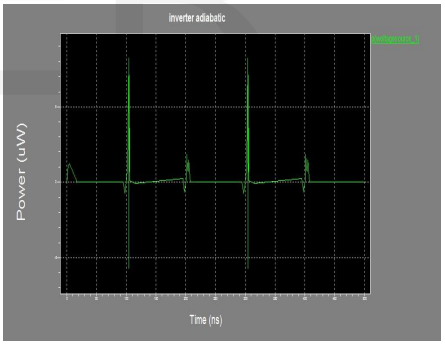


Fig.25 Waveform for Power of Adiabatic CMOS Inverter

B. **NAND Gate**

Operation When A=0 and B=0, both the nMOS transistors are OFF and both pMOS are ON. Hence, the output is connected to VDD and we get logic high at the output .When A=1 and B=0, the upper nMOS is ON and lower nMOS is OFF, so the output cannot be connected to the ground. Under this condition left pMOS is OFF but right pMOS is ON. Hence, the output is connected to VDD we get logic high at the output. When A=0 and B=1, the upper nMOS is OFF and lower nMOS is ON, so the output cannot be connected to the ground. Under this condition left pMOS is ON but right pMOS is OFF. Hence, the output is connected to VDD we get logic high at the output. When A=1 and B=1, both the nMOS transistors are

ON and both the pMOS transistors are OFF. Hence the output is connected to the ground and we get logic low at the output.

Different W/L Ratio

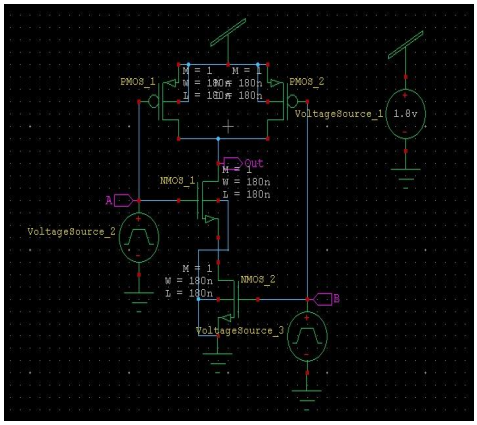


Fig.26 1:1 Ratio CMOS NAND Gate

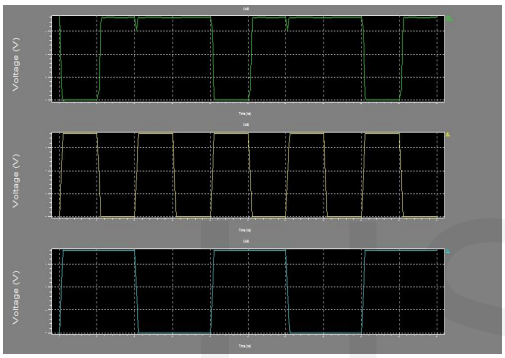


Fig.27 Waveform for Voltage of 1:1 Ratio NAND Gate

Fig.28 Waveform for Power of 1:1 Ratio CMOS Inverter

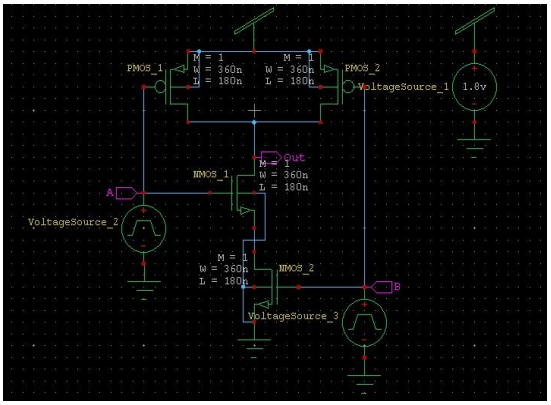


Fig.29 2:1 Ratio CMOS NAND Gate

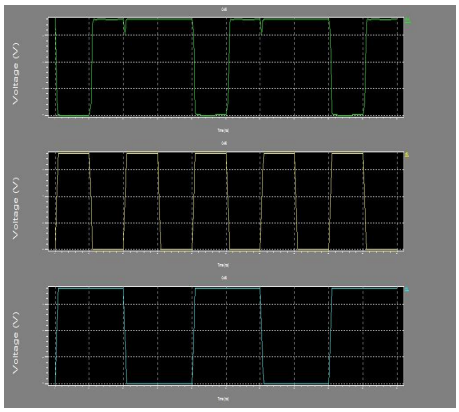


Fig.30 Waveform for Voltage of 2:1 Ratio NAND Gate

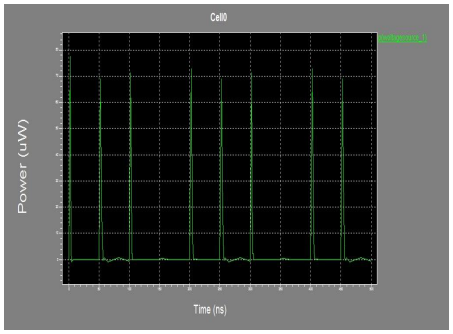


Fig.31 Waveform for Power of 2:1 Ratio CMOS Inverter

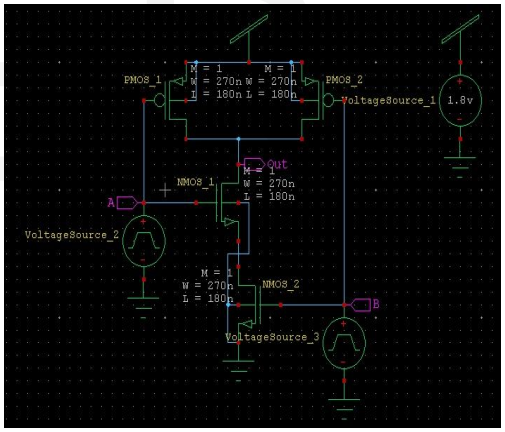


Fig.32 3:2 Ratio CMOS NAND Gate

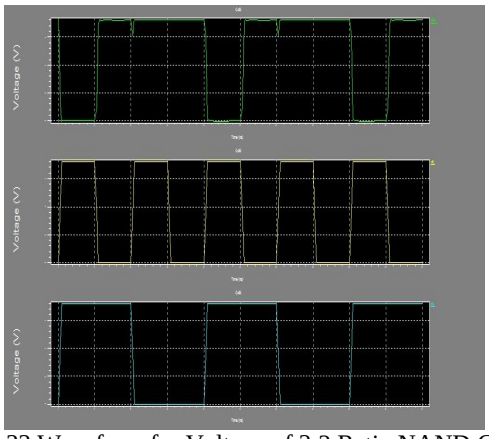


Fig.33 Waveform for Voltage of 3:2 Ratio NAND Gate

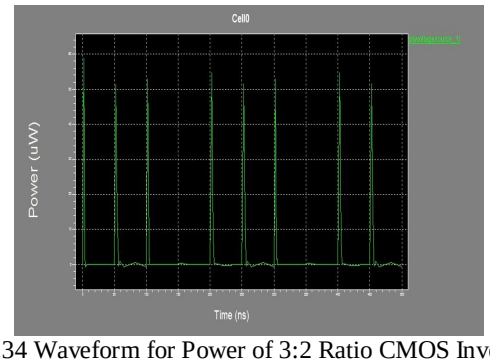


Fig.34 Waveform for Power of 3:2 Ratio CMOS Inverter

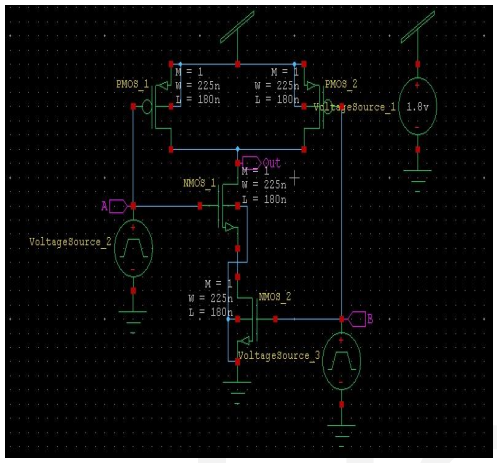


Fig.35 5:4 Ratio CMOS NAND Gate

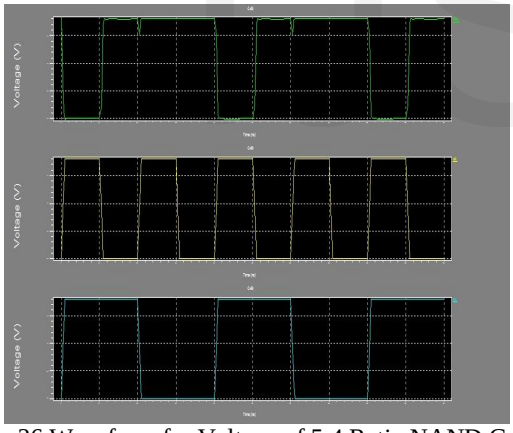


Fig.36 Waveform for Voltage of 5:4 Ratio NAND Gate

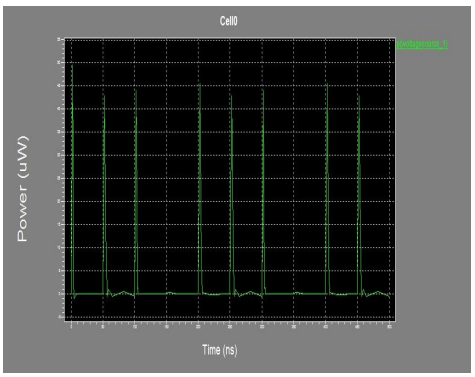


Fig.37 Waveform for Power of 5:4 Ratio CMOS Inverter

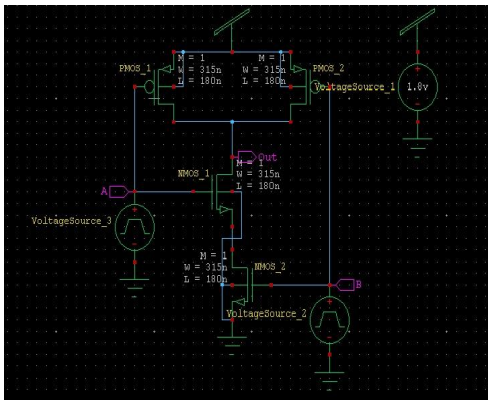


Fig.38 7:4 Ratio CMOS NAND Gate

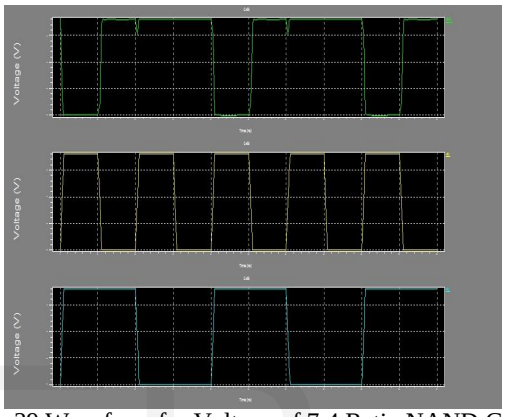


Fig.39 Waveform for Voltage of 7:4 Ratio NAND Gate

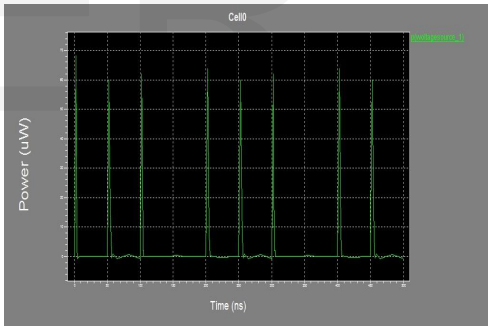


Fig.40 Waveform for Power of 7:4 Ratio CMOS Inverter

Conventional

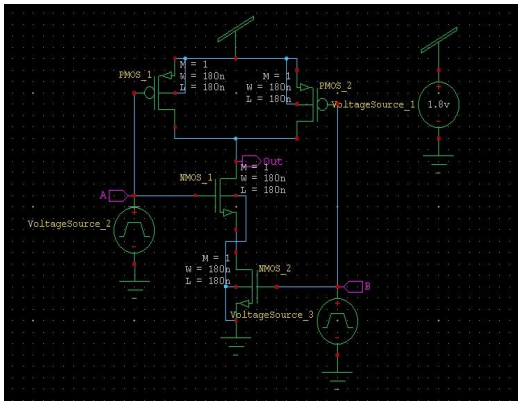


Fig.41 Conventional COS NAND Gate

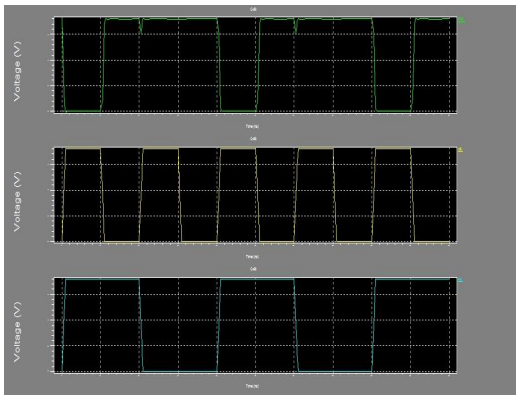


Fig.42 Waveform for Voltage of Conventional NAND Gate

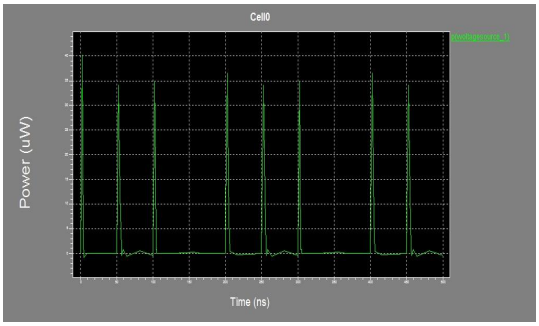


Fig.43 Waveform for Power of Conventional CMOS Inverter

Stacking

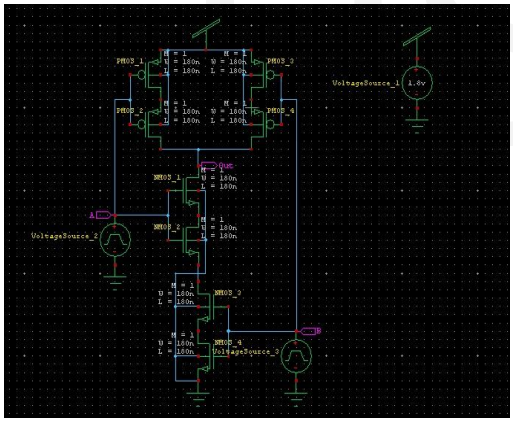


Fig.44Stacking CMOS NAND Gate

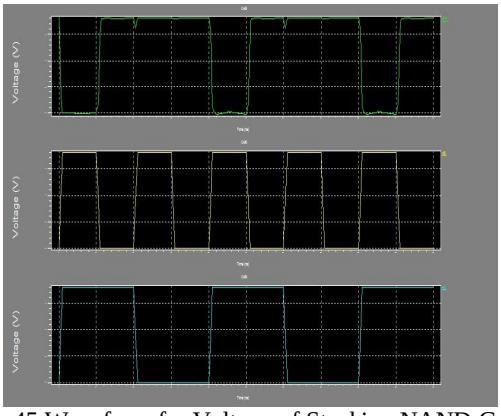


Fig.45 Waveform for Voltage of Stacking NAND Gate

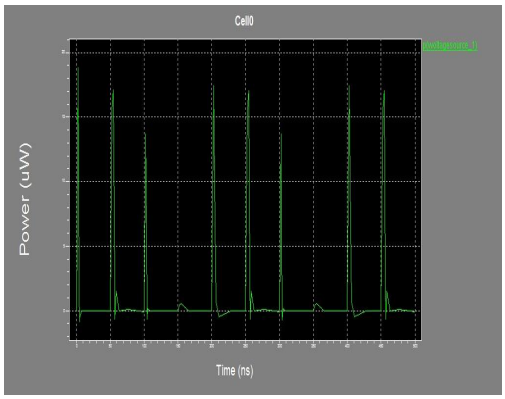


Fig.46 Waveform for Power of Stacking CMOS Inverter

Adiabatic

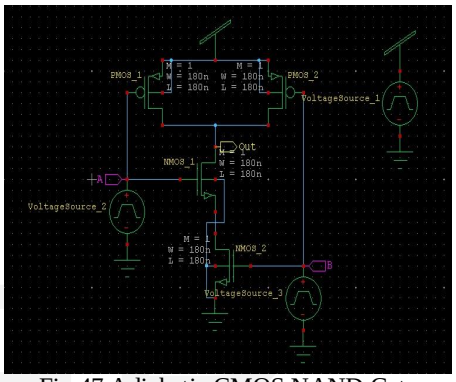


Fig.47 Adiabatic CMOS NAND Gate

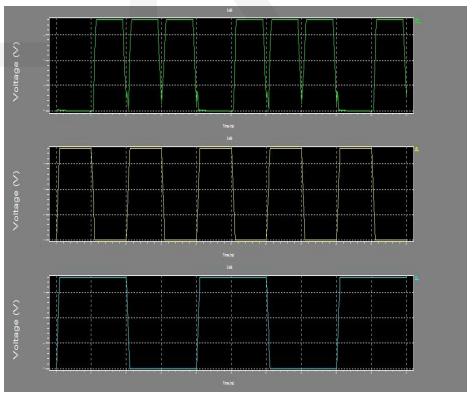


Fig.48 Waveform for Voltage of Adiabatic NAND Gate

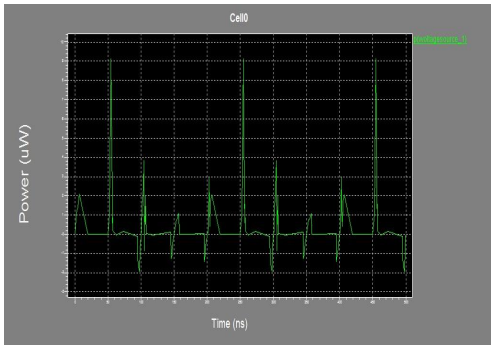


Fig.49 Waveform for Power of Adiabatic CMOS Inverter

VI. RESULT ANALYSIS

The Simulation of logic gates with and without low power techniques is carried out at 180nm, technology. CMOS technology parameters are taken for NMOS and PMOS transistors, using Tanner tool. Transient Analysis is done to get Delay and Average Power results.

We have studied different width and length ratio and compare the power consumption for different width and length ratio.

TABLE 1 CMOS NOT GATE RESULT

WIDTH / LENGTH Ratio	AVERAGE DELAY (In Nano Second)	AVERAGE POWER CONSUMPTION (In Microwatt)
1 : 1	0.1496	0.8384
2 : 1	0.1394	1.5833
3 : 2	0.1428	1.2093
5 : 4	0.1455	1.0232
7 : 4	0.1409	1.3960

TABLE 2 CMOS NAND GATE RESULT

WIDTH / LENGTH Ratio	AVERAGE DELAY (In Nano Second)	AVERAGE POWER CONSUMPTION (In Microwatt)
1 : 1	24.721	1.5270
2 : 1	24.752	2.9587
3 : 2	24.741	2.2453
5 : 4	24.733	1.8857
7 : 4	24.747	2.6022

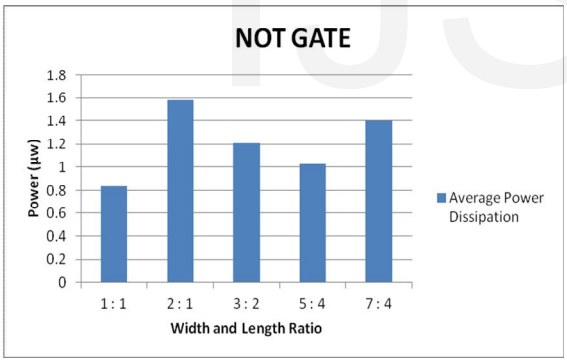


Fig.50 Comparison of Average power for NOT Gate using different W/L Ratio

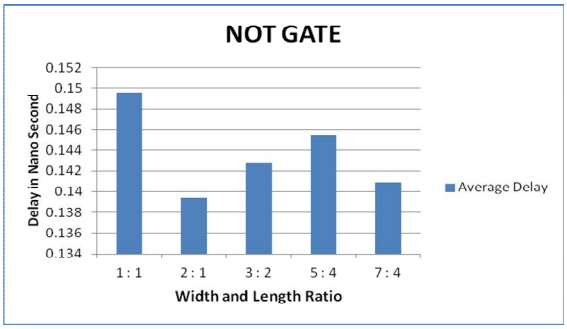


Fig.51 Comparison of Average Delay for NOT Gate using different W/L Ratio

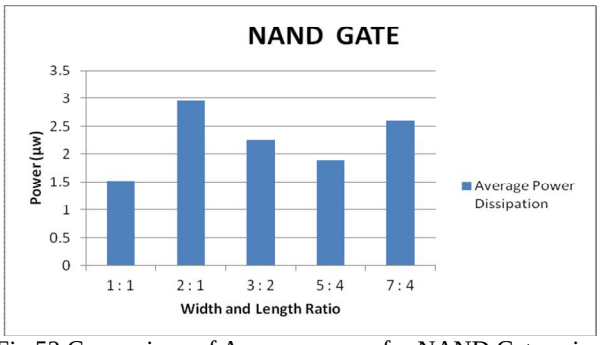


Fig.52 Comparison of Average power for NAND Gate using different W/L Ratio

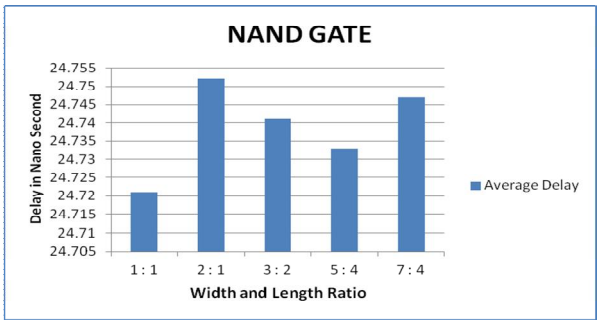


Fig.53 Comparison of Average Delay for NAND Gate using different W/L Ratio

TABLE 3 CMOS NOT GATE RESULT

POWER REDUCTION TECHNIQUE	AVERAGE DELAY (In Nano Second)	AVERAGE POWER CONSUMPTION (In Microwatt)
Conventional	0.1496	0.8384
Adiabatic	98.061	0.1084
Stacking	0.8251	0.4603

TABLE 4 CMOS NAND GATE RESULT

POWER REDUCTION TECHNIQUE	AVERAGE DELAY (In Nano Second)	AVERAGE POWER CONSUMPTION (In Microwatt)
Conventional	24.721	1.5270
Adiabatic	23.554	0.2731
Stacking	24.619	0.8842

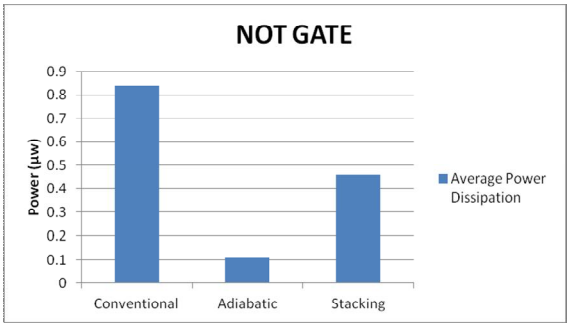


Fig.54 Comparison of Average power for NOT Gate using different Techniques

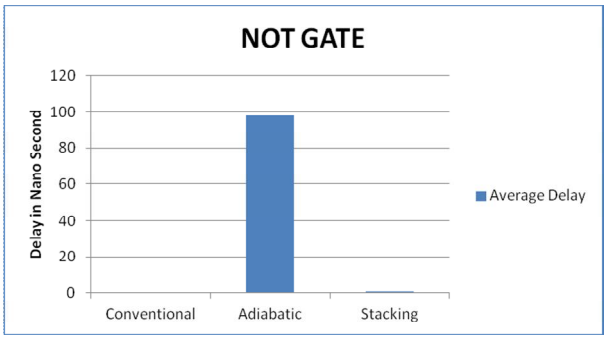


Fig.55 Comparison of Average Delay for NOT Gate using different Techniques

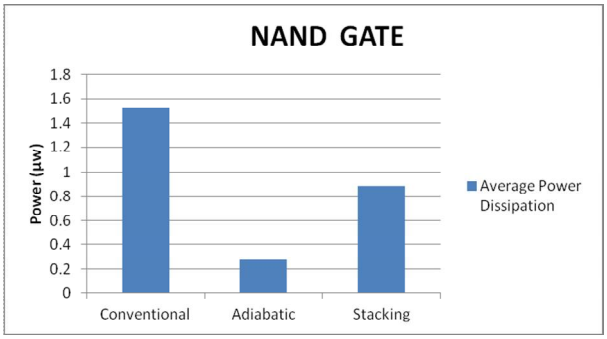


Fig.56 Comparison of Average power for NAND Gate using different Techniques

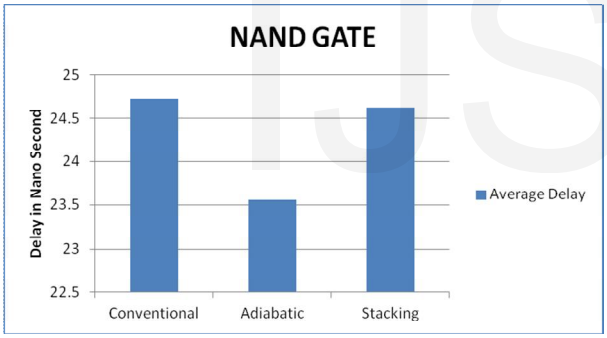


Fig.57 Comparison of Average Delay for NAND Gate using different Techniques

VII. CONCLUSION

Comparison has been done for NOT & Nand Gates , delay and power is calculated for Different Width and Length Ratio. Implementing the Different Width and Length Ratio, we can observe that minimum power consumed in 1 : 1 ratio.

After finding the result for different width & length ratio, we use that result and design the NOT & NAND Gate using Conventional, Adiabatic & Stacking Techniques. Implementing these techniques for power reduction than we can observe that Minimum power consumed in Adiabatic Technique. The tool for simulation is TANNER and at 180 nm technology and the practical observations has been tabled

REFERENCES

[1] Robert Rogenmoser, Hubert Kaeslin and Norbert Felber, “Impact of transistor sizing on power efficiency in submicron cmos circuit”, Integrated systems laboratory swiss fedral institute of technology ch-8092, zurich, Switzerland.

[2] Anantha P Chandrakasan and Robert W Broderson, Fellow “Minimum power consumption in digital cmos circuit”, proceeding of IEEE, vol 83, n0.-4, april 1995.

[3] N Whein and M Munch “Minimum power consumption in digital circuits and systems”, university of Kaiserslouterm, Germany.

[4] Krashna Nand Mishra”Efficient Carry Generation technique Incorporating Energy Recovering Logic Circuitry For Low Power VLSI.” IEEE, 2008

[5] Y. Moon and D. K. Jeong, “An efficient charge recovery logic circuit,” IEEE Journal of Solid-State Circuits, vol. 31, no. 4, pp. 514–522, 1996.

[6] P. Kalyani, Dr. P. Satish Kumar, Dr. KRagini, “Various low power techniques for CMOS circuits”, International journal of engineering research and applications, ISSN: 2248-9622, vol.3, issue 6, nov – dec 2013, pp 330 – 333.

[7] Neha Goyal, Renu Singla, Puneet Goyal, “study & analysis of universal gates using stacking low power technique:, International journal of computer science & Information technologies, vol 6(3), 2014, pp 4200-4204.

[8] Kapil Mangla, Neha Mangla, “ Power dissipation of combinational circuits by adiabetic techniques for 180nm CMOS technology” IJLTEMAS, vol.3, issue 6, june 2014.

[9] Renu Singla, Puneet Goyal, Neha Singla, “ Comparative study and analysis of universal gates for minimizing power and delay using lector techniques” IJARCS, vol. 5(5), may – june-2014, pp 29-33.

[10] Neil H.E.Weste, David Harris, Ayan Banerjee “cmos VLSI Design (a circuit and system perspective)”, Pearson Education Publication.

[11] Robert L. Boylestad, Louis Nasheslsky “electronics device and circuits” Pearson Education Publication.

[12] Kamran Eshraghain, Douglas A Pucknell, Sholeh Eshraghian “Essential of VLSI circuits and systems”, PHI Publications.

[13] [Online].Available:http://docencia.ac.upc.edu/master/ MIRI/NCD/as signments/Tema%201-EN.pdf.