Design and Simulation of Silicon Nanowire Transistor Using TCAD

Pawan Rewatkar, Saurabh Joshi

Abstract— we present a paper on simulation study of silicon nanowire transistor base on the solution self consistent of Poisson, Schrodinger and continuity equation on three dimensional domain. The final device was enhanced for both high performance and low operating power application. A advance study on future technology nodes down to the 14nm node was performed which showed short channel effect. A process variation study was accompanied in comparison with a finFET device. A silicon nanowire FET displays less sensitivity to process variation. To simulation for this device correct modeling and calculations based on quantum mechanics theory are necessary. The use of a mode space approach (either coupled or uncoupled) yields high computational efficiency that makes our three dimensional quantum simulator practical for extensive device simulation and design.

Index Terms— 3-D Schrodinger equation, 2-D NEGF, Poisson equation, continuity equation, Threshold voltage, drain-induced-barrier-lowering (DIBL), FinFET, Silvaco TCAD,
.

1 INTRODUCTION

As the standard silicon metal oxide semiconductor earth result transistor (MOSFET) ways its scaling limits, many new (original) device structures are being extensively explored. To comprehend mechanism physics in depth and to assess the presentation limits of SNWT simulation is becoming increasingly important. A complete 3-D self consistent ballistic SNWT simulator has been established on the basis of effective mass approximation. The silicon nanowire transistor has been obtain broad attention from both the semiconductor and academia. Nanowire transistor can be made using different material on low cost substrates such as glass or plastics. Si and Ge nanowire transistor are of particularly more importance because of their mutual interference with CMOS technology. Reducing future size and new device designs increases the need for that we use TCAD software. This offers a approach to strong 3D process simulation.

2 Review Stage

2.1 The Initial of Silicon Nanowire Transistors

The Initial of Silicon Nanowire Transistors Integrated Circuit technology has been considered as one of the most important inventions in engineering history. The incredible progress in IC technology in the past 4 decades has become the driving power of the Information Technology (IT) revolution, which has impressively changed our lives and the complete world. The secret of the vision in IC technology is actually simple: scaling down the dimension of each transistor.

The basic element of ICs, and increasing the total number of transistors in one IC chip. The device scaling has been successfully predicted by Moore's law –This law state that the processor speed or overall processing power for computer will double every two year of several digital electronic devices are strongly connected to morre's law[6].. To date, microprocessors with >100 million transistors have been realized, and the corresponding MOSFET gate lengths in modern Integrated Chips chips have entered the sub-100nm regime. Continuous success in device scaling is essential for maintaining the successive improvements in IC technology. As the MOSFET gate length enters the nanometer regime, however, short channel effects (SCEs), such as threshold voltage (*VT*) roll off and drain-induced-barrier-lowering (DIBL), become progressively significant, which limits the scaling capability of *planar* bulk or silicon-on-insulator (SOI) MOSFETs. At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance (e.g., ON-current and intrinsic device delay). For these explanations, various novel device structures and materials – silicon nanowire transistors, carbon nanotube FETs, new channel materials, molecular transistors. Among all these promising post-CMOS structures, the silicon nanowire transistor (SNWT) has its unique advantage – the SNWT is based on silicon, a material that the semiconductor industry has been working on for over 30 years; it would be really smart to stay on silicon and also achieve good device metrics that Nanoelectronics delivers. As a result, the silicon nanowire transistor has obtained wide attention from both the semiconductor industry and academia. According to the fabrication technology, newly reported Silicon Nanowire Transistors can be classified into two groups:

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1) The first-type SNWTs can be viewed as 'narrow-channel' SOI MOSFETs realized by using a 'top-down' approach. Different from planar SOI FETs, the channel (Si body) widths of SNWTs are lithography-defined and similar to the Si body thicknesses therefore the gate stacks are permitted to wrap around the wire channels to realize multi-gate or gate-all-around FETs, which offer better gate control than planar MOSFETs. In current experimental SNWT structures, the wire dimensions (i.e., Si body thickness and width) range from 10nm to 100nm. At the scaling limit, where the gate length of device is maybe shorter than 10nm, this dimension has to be scaled down to the sub-10nm regime to maintain good electrostatic integrity. To sort out this, very-high resolution lithography (e.g., <5nm) is required to define the nanowire widths. Therefore, the ultimate scaling of the top-down SNWTs could be limited by the highest resolution of lithography that can be reached in training. It should also be noted that the smallest lithography defined length in the circuits based on the top down Silicon Nanowire Transistors should be the SNWT channel (Si body) width instead of the transistor gate length.[10].

2) To avoid very-high-resolution lithography in the fabrication of Silicon Nanowire Transistor, a number of experimental groups are trying to synthesize semiconductor (e.g., Si, Ge, and GaN) nanowires by using 'bottom-up' approaches, such as the Vapor-Liquid-Solid (VLS) growth technique. With this technology, single-crystal Si nanowires with a diameter as small as 2-3nm have been achieved. Based on these bottom-up nanowires, various types of devices and circuit components have been experimentally demonstrated, e.g., field-effect transistors (FETs), nanowire heterojunctions, logic gates, memory , decoders , bipolar transistors , thin-film transistors , light emitting diodes (LEDs), lasers , photodetectors , and nanosensors. For the FET application, the bottom-up technique offers a possible, low-cost solution to achieve nanowires with ultra-small diameters and relatively smooth interfaces, which are essentially important for scaling the transistor gate length below 10nm[10]. Semiconductor nanowires (NWs) and carbon nanotubes (NTs) are striking components for future nanoelectronics since they can shows a range of device function and at the same time serve as linking wires that connect to larger scale metallization. For example, field effect transistors (FETs) have been configured from NWs and NTs by depositing the nanomaterial on an insulating substrate surface, making source and drain contacts to the NW or NT ends, and then configuring either a bottom or top gate electrode. This basic approach may serve as the basis for hybrid electronic systems consisting of nanoscale building blocks integrated with more complex planar silicon circuitry, although a number of issues including device performance, reproducibility, and integration will have to be addressed in order to realize such systems in the future.

In brief, the rapid progress in nanofabrication technology has shed light on the use of silicon nanowire transistors in future electronics. Consequently, understanding device physics of SNWTs and developing TCAD (Technology Computer Aided Design) tools for SNWT design become progressively important. The *principle objective* of the paper is to theoretically see the sights device physics of silicon nanowire transistors by doing computer-based numerical models. With the simulation tools we develop, we will subsequently assess the ultimate performance limits of SNWTs and address the important issues in Silicon Nanowire Transistor device design.[10]

2.2 Ballistic Transport

In semiconductor three dimensional simulation domain obeys the Poisson equation.

$$\nabla[\in(r)\nabla\emptyset(r)] = q(p - n + N_D^{\ +} + N_A^{\ -}) \text{------------------(1)}$$

Where $\emptyset$ is electrostatic potential, $\in$= the dielectric constant, q=elementry charge, n & p= free electron and free hole concentration, $N_D^{\ +}$= concentration of donar ion and $N_A^{\ -}$= concentration of acceptor ion. In the 3D domain full stationery Schrödinger equation is given as-

$$H_{3D}\,\psi\,(x,y,z) = E\psi(\,x,y,z) \text{-----------------------------(2)}$$

Where H_{3D} is the 3D device Hamiltonian [5]. Assuming an ellipsoidal parabolic energy band with a diagonal effective mass tensor, H_{3D} defined as,

$$H_{3D} = -\frac{\hbar^2}{2m_x^*(x,y)}\frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{2m_y^*(y,z)}\frac{\partial}{\partial y}\right) - \frac{\hbar^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{2m_z^*(z,x)}\frac{\partial}{\partial z}\right) + U(x,y,z) \text{-----------(3)}$$

Here m_x^*, m_y^* and m_z^* are the electron effective masses in the x, y, z direction respectively, and *U(x, y, z)* is the conduction band-edge shape due to the electrostatic potential in the active device. Since the wave functions reduce quickly from the confining potential barriers in the equation of Schrödinger solutions, the carrier concentrations become small and noisy.[2][8] Transport in SNWT is then likely to be in an intermediate regime between fully ballistic and drift-diffusion transport. Dissipative transport can be addressed in a quantum framework as in [9] by means of the Büttiker probes approach, which corresponds to the approximation of a single energy-independent relaxation length, by the definition of self-energies, which account scattering within the NEGF formalism [14], or following an approach similar to that proposed in [15], where drift-diffusion transport in planar MOSFETs is computed in each 2-D sub band. We believe the latter approach can provide, with relatively reduced computational resources, relevant information on the degradation of performance with respect to the

ballistic case. The actual device will exhibit performance intermediate between the two limiting cases of ballistic and drift-diffusion transport

2.3 Capacitance Extraction of SNWT

To evaluate the field effect mobility, simulation of TCAD was done by Silvaco TCAD. This can estimate the capacitance more accurately than any analytical formula. Here Poisson equation was solved together with drift diffusion equation to solve the electrostatic profile. For the correct simulation. We did a comparative analysis why TCAD simulation for NW capacitance extraction method is better than the analytical formula based formula for cylindrical shape object quite accurate result, but our top gate does not cover the NW extraction. Even though analytical for capacitance of cylindrically rather 80% of the circumference of the NW is covered .Thus analytical formula below gives incorrect estimation of capacitance.

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}(1+\frac{2t_{ox}}{d_{nw}}} \quad \text{--------------------------(4)}$$

3 Software Simulation

The simulation software used for nanoscale nanowire transistor is TCAD [16]. The tool (NanoWire) is a 3-D self consistent, silicon nanowire simulator based on the effective-mass approximation. The calculation contain a self consistent solution of 3-D Poisson equation and a 3D Schrödinger equation with open boundary conditions at the source and drain contacts. Using the finite element method (FEM), the 3-D Poisson equation is solved initially to obtain the electrostatic potential throughout the device. At the same time, the 3-D Schrödinger equation is solved by a mode space approach, which offers both computational efficiency and high accuracy as compared with through real space calculations. we present the simulation of a silicon nanowire transistor (SNWT), whose structure is shown in Fig. 1, with channel length L = 7 nm and In our simulation, a single number (N = 1) of dopant with diameter of 1 nm and the corresponding N_A of 1.9 × 1021 cm-3 are assumed. The channel diameter and channel length are in multiple of l's (e.g., L = 7 nm and D = 4 nm), and x-z plane (cross section) of the silicon wire. Here, quantum confinement arises in the x and z directions while transport in 1-D sub-bands in the y direction. For such geometries, one dimensional sub-bands are well separated, so transport can be considered independently in each sub-band. We have considered a fully ballistic transport in the channel, both in the semiclassical and in the quantum case (i.e. considering barrier tunneling), and, in addition, we have solved the drift/diffusion equation in each 1D subband taking into account velocity saturation: in this way we have been able to define an upper (fully ballistic transport) and a lower limit (drift/diffusion transport) for the device performance, as well as to study the influence of quantum transport on device characteristics. In Fig. 3 we plot the transfer characteristics of SNWT device.

Simulation of electronic devices generally involves self consistent solution of the electrostatic potential and carrier distribution inside the device. Over the years device engineers have improved our collective knowledge of carrier transport and semiconductor physics. Earlier treatment of electrons and holes as semiclassical particles with an effective mass was good enough to predict semiconductor device behavior and the drift diffusion equation was adequate to describe carrier transport. Today, as we stand at 65 nm node and begin to enter 45 nm technology node, MOSFETs have shrunk to nanoscale dimensions, which has required a re-examination of our approach to device modeling. In particular, the properties of materials can be altered using strain, heterojunctions and computational grading are possible, and quantum effects start to show up in the nanometer regime. As a result, the conventional drift-diffusion and Boltzmann equations do not capture the increasingly important role of quantum mechanics in modeling transistors in the ten nanometer regime. For this reason, a more sophisticated analysis of the device physics is needed, such as the non equilibrium Green's Function (NEGF) approach, to model devices all the way to ballistic level (< 10 nm) [1]. The NEGF transport model is by far the most rigorous approach among existing quantum transport models and is the approach utilized in this modeling study

3.1 Figures

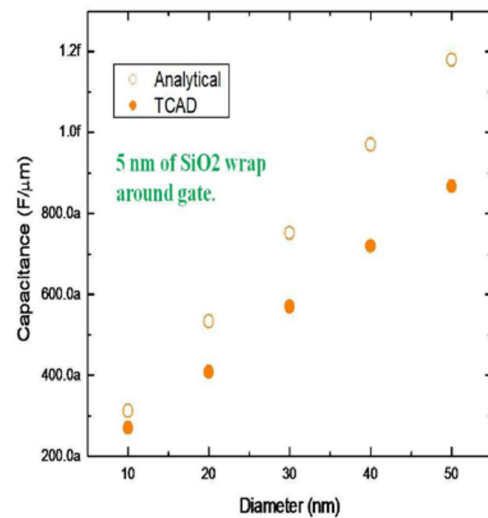

Fig.1 The comparison between analytical formula and TCAD based estimation. [7]

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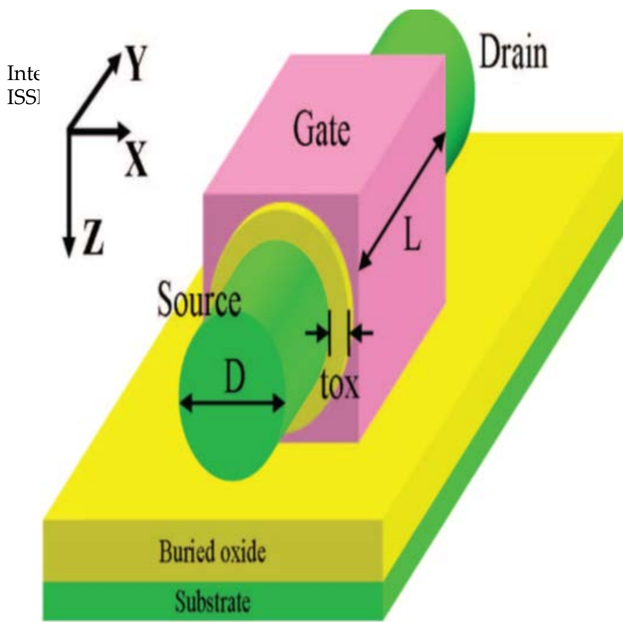

Fig. 2. 3-D view of nanowire transistor device where y axis is in the direction along the channel and x-z surface corresponds to the cross section of the wire. [3]

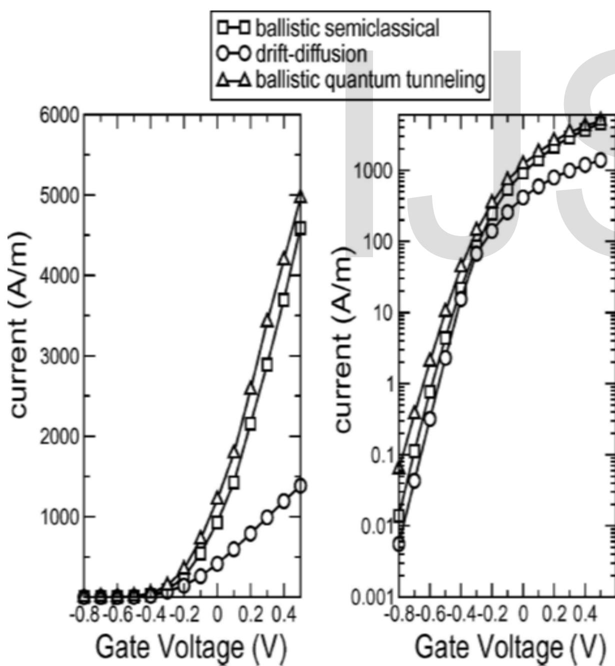

Fig3. Transfer characteristics of the SNWT device with L=7nm in the linear and in the logarithmic scale. [3]

3.2 Analysis

A three dimensional device simulation based on the self-consistent Schrodinger–Poisson's equation is used for only the mobile charge i.e. electron. It is calibrated by 2D Non-Equilibrium Greens Function (NEGF) transport equation in mode space to find out quasi-Fermi level of electron. Here, a 2D NEGF Mode Space (NEGF MS) transport simulation is used in the confinement direction (*XY* plane) as a slice of the Si body. First, created a mesh. A spacing in the transport association ought to be fine. Due to a ballistic nature of transport, near the source and drain contacts no voltage drop. Moreover, the potential in the drain and source has to be allowed to float because some electrons are reflected retrograde and thus total carrier concentration in contacts can change alongside bias. For these reasons we apply von Neumann boundary conditions for potential at the contact. However, Fermi levels in contacts are fixed. Schrodinger equation will be solved in each part of the device. *NEGF-MS* parameter identifies that we need to calculate transport with Non-Equilibrium Greens Function (NEGF) way in the mode (subband) space. The coupling is forceful adjacent wide-narrow span interface. A parameter NEGF-CMS in its place of NEGF-MS will impose coupled mode space approach. This slice is pulled towards the *z* direction for full band quantum simulation. In this simulation, only the gate length and body width have been taken as parameters. Device scaling as well as its gate length scaling becomes the most important parameter.

Conclusion

In this paper, we want to stress the fact that nanowire transistor simulation tool represents a significant advantages with respect to the state of art. We also believe that the approximation which we took are very good tradeoff between accuracy and computational resources. From the above discussion it infers that the silicon nanowire transistor are less sensitive. The SNWT shows the superior short channel effect. The experimental result indicates that nanoscaled SNWT can be one of the most promising structure nanowire field effect device. The nanowire diameter designed at 2/3rd of gate length minus three times gate oxide thickness was shown to achieve good control of short-channel effects.This model has been broadly verified by 3-D numerical simulation and demonstrated to be accurate enough for most circuit simulation. Further extensions, such as introducing limited intersubband scattering via a generation-recombination term, or including a more sophisticated mobility model, or even an energy-balance model per subband, can be done substantially without modifying the code structure.

Future Work

The current transport model used for simulations assumes a ballistic transport that is carrier transport without any scatter-

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ing in the channel. A more accurate transport model could be used bringing into account the surface scattering effects, which start to dominate at very small diameters (<5 nm). Also the simulation software assumes an ideal wrap around gate for the nanowire FET. Since this ideal structure is not possible in practice, changes can be incorporated into the device structure to more faithfully reproduce the actual device structure. Further work could be done by simulating nanowire FET with new materials such as SiGe nanowire channel and high-k dielectrics.

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