Modelling of On Current In a Scaled MOSFET Considering the Effect of Saturation Velocity and Temperature

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Abstract. **The metal oxide semiconductor field effect transistor is the building block of VLSI(Very Large Scale Industry).Minimum featrure size of the ICs has shurnk consideably over the time of several decades. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area.As a consequence,the number of transistor has increased over time. When gatelength is scaled into nanoscale , second order effects are becoming a dominant issue to be dealt with in transistor design. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. Accurate description of temperature effects in a device is necessary for a circuit level MOSFET model to predict circuit behaviours over a range of temperature. This paper analysis the limiting effects of saturation velocity on drain current and scaling of the on-current temperature effects in MOSFET devices.It is concluded that temperature dependence decreases with technology scaling.**

Key word:VLSI.MOBILITY.VELOCITYSATURATION , MOSFET,SCE,DIBL,CLM,SOE.

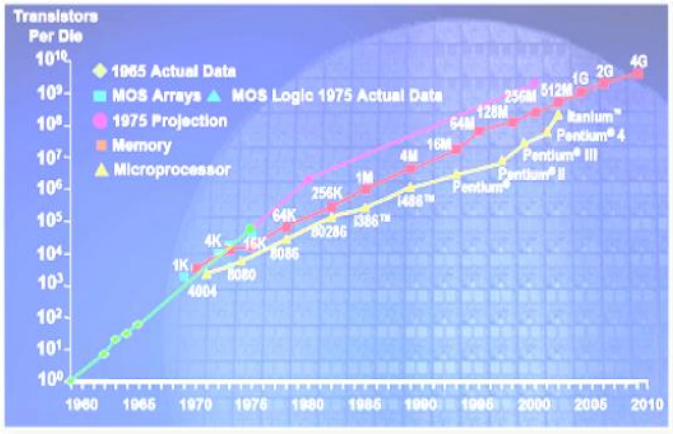
I. INTRODUCTION

Metal oxide semiconductor field effect transistor is the workhorse of the Integrated Circuit Technology.A vast majority of contemporary silicon chips use the MOSFET as the active component. MOSFETs dimensions have continuously shrink in order to realize higher speed & packing density. When miniaturizing MOS field-effect transistors (MOSFETs) for their high degree of integration, a source and a drain come close to each other, and the drain field has an effect on the source. The phenomenon, called "short channel effect," which miniaturizing MOS field-effect transistors (MOSFETs) for their high degree of integration.Which deteriorates device performance. Progress in scaling of MOS transistors and integrated circuits over the years is reviewed and today's status and challenges are described in [1]. Where channel length L is comparable to the depletion widths associated with the drain and source. The change in operation temperature will influence the characteristics of a device and its performance.

The paper includes a theortical analysis of the scaling of the MOSFETs in Section II. Temperature dependences of saturation velocity and mobility in section III .The limiting effects of velocity and the temperature impact on drain current are examined in secton IV. Finally, some conclusions are provided in Section V.

II. THEORY

Semiconductor memories and microprocessors are two major filelds ,which are benefited by the growth in semiconductor technology. Gordon Moore made his observation in 1965 .He observed an exponential growth in the number of transistors per integrated circuits in which the number of transistors nearly doubled every couple of years.This observation known as Moore's law still holds true today. The "Moore's Law" is a succinct description of the persistent periodic increase in the level of miniaturization in fig(1).



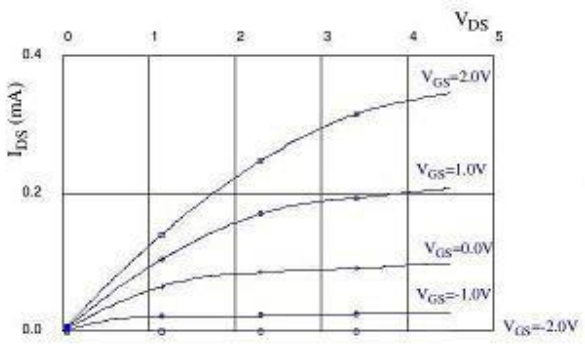
Fig(1) The growth of semoconductor technology

As MOSFET channel length is reduced, the device threshold becomes dependent on L and V_{DS}. These deviations from the ideal threshold model are known as the short channel effects.The limitation on electron drift characterstics and the modification of the threshold voltage are the major physical phenomena due to short channel effects.Scaling of MOS dimensions is important in order to improve the drivability, and to achieve higher-performance and higher-functional VLSI's. When the channel length shrinks, the controllability of the gate over the channel depletion region reduces due to the increased charge sharing from source/drain.

In long channel,edge effects from the four sides can be neglected .Channel length L must be much greater than the sum of the drain and source depletion width .
For a long channel transistor the charge

$$\left[Q_{BL} = -qN_A \frac{ZLW_{max}}{ZL} - qN_A W_{max} \right] \quad (1)$$

Where Z is the width of the device
The I_D V_{DS} characterstic of a long channel NMOSFET is shown below in figure(2)



Fig(2) .The ouput characterstics of a long channel NMOSFET keeping V_{GS} as constant

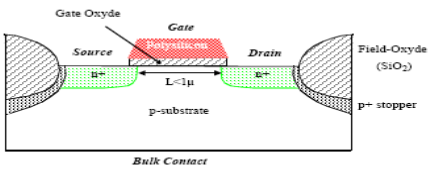
T he drain current in linear region and in saturation region is given by equatrion no(2) and (3) When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$ and When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$ is

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (2)$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda (V_{DS} - V_{DSsat})) . \quad (3)$$

where $\mu_n$is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area.λ is the channel length modulation parameter .In saturation, current is independent of V_{DS} and increases as the square of V_{GS}. This is termed "square law" behavior. In saturation, a MOSFET is an ideal current source. current does not depend on V_{DS}.

When gatelength is scaled second order effects are becoming a dominant issue .We can say that the story of MOSFET scaling is the history of how to prevent short-channel effects (SCE) as in [2]. SCE degrades the controllability of the gate voltage to drain current, which leads to the degradation of the sub threshold slope and the increase in drain off-current.. The cross section of in short channel MOSFET is in fig(3)



CROSS-SECTION of NMOS Transistor

Fig(3) NMOS Transistor with channel length less than 1µm

With the reduction of channel length, control of short-channel effects is one of the biggest challenges in further scaling of the technology. The predominating short-channel effects are a shift in threshold voltage and a lack of pinch-off with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage. Thinning gate oxide and using shallow source/drain junctions are known to be effective ways of preventing SCE.In short channel device the length L is reduced to increase both the operation speed and the number of components per chip .

The charge in trapezoidal region is given by

$$Q_{BS} = -qN_A W_{max} \frac{L + L'}{2L} \quad (4)$$

Where N_A is sudstrate acceptor impurities.In short channel the current from drain to source in saturation region is modeled as

I_D= W Vsat Cox(V_{GS}-V_{THN}-V_{Dsat}) (5)

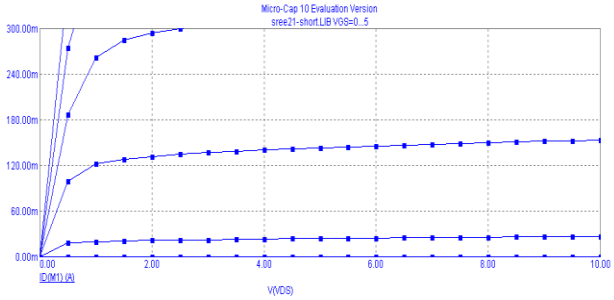
and threshlod voltage is given by (6)

V_{TO}= V_{T0}(longchannel) - ΔV_T (6)

Where ΔVT is the reduction threshold voltage

$$\Delta V_T = -\frac{qN_A W_{max}}{C_i} \left(1 - \frac{L + L'}{2L} \right)$$

The I_D-V_{DS} chara of a short channel NMOS is shown below in figure(4)



Fig(4).output chara of a short channel NMOSFET keeping V_{GS} constant

It shows that, those devices with smaller geometry have higher drain currents; hence devices with smaller geometry have lower threshold voltages. The threshold voltage of a MOSFET is defined as the gate voltage where an inversion layer forms at the interface between the insulating layer and the substrate of the transistor. A new analytical threshold voltage roll-off equation for MOSFET by effective-doping model is proposed by [3].Young [4] analyzed the SCE using a device simulator, and concluded that SCE is well suppressed

in thin-film SOI MOSFET's when compared to bulk MOSFET's.

III.TEMPERATURE DEPENDENCE OF MOBILITY AND SATURATON VELOCIY

For very short channel devices, electron velocity overshoot is expected to take place for channel length below 0.1um.

When a strong enough electric field is applied in a semiconductor , the carrier velocity in the semiconductor reaches a maximum value, called saturation velocity .

Above the critical field the mobility start to decrease where as below critical field mobility essentially constant.New mobility degradation specific to short channel MOSFETs is studied and elucidated as in[5].

The drain current is expressed interms of velocity and mobility as

$$Id = -\upsilon(x)Q(x)\,W = -\mu\varepsilon(x)\,Q(x)\,W \qquad (7)$$

The carrier velocity is empirically related to the mobility through

$$\upsilon = \mu\varepsilon(x) \qquad (8)$$

Hence current increase linearly with the lateral electric field between source and drain.

$$\varepsilon_{lat} = Vds/L \qquad (9)$$

where W is the width of the channel and υ and Q are the carrier velocity and the induced charge per unit area at point x , ε is the electric field across the channel length.

Thus the saturation current without velocity saturation as in(10)

$$I_{ds}=\frac{\beta}{2}(V_{gs}-V_t)^2 \qquad (10)$$

changes to the equation below if the transistor were completely velocity saturated is given as(11)

$$I_{ds}=C_{ox}W(V_{gs}-V_t)\,\upsilon_{sat} \qquad (11)$$

Thus current is linearly dependent rather than quadratically dependent.However the velocity saturation and mobility share the same temperature dependence only until velocity saturation occures .As in [13] after the critical filed ,the carrier velocity saturates to a constant value and from that point on ,an increase in the electric field does not result in the carrier velocity higher than the saturated value.

The temperature dependence of the carrier mobility is given by eq(12)

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \qquad (12)$$

Where T is the junction temperature ,T_0 is the nominal temperature ,which is equal to the room temperature (298K).Temperature coefficent θ is ideally 1.5.The temperature dependence of the saturation velocity can be written as in (13)

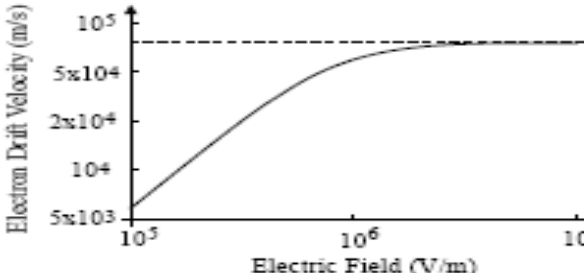
$$\upsilon_{sat}(T) = \upsilon_{sat}(T_0) - \eta(T - T_0) \qquad (13)$$

Where η is the temperature coefficient whose value is extracted to be around $150ms^{-1}\,K^{-1}$ .The saturation velocity has a more linear relation ship with temperature.

IV. RESULTS AND DISCUSSIONS

.1.The limiting effect of velocity on drain current in scaled device.

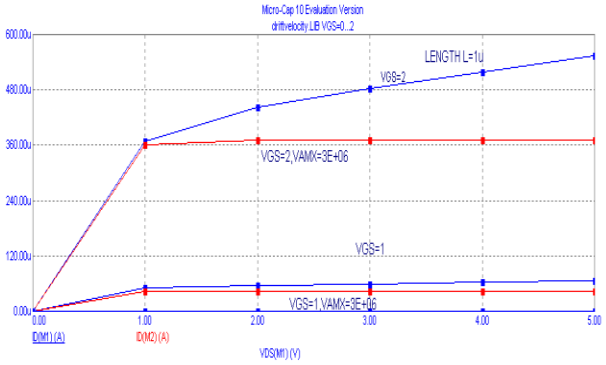
At low electric field ,the drift velocity of electron ,Vd is proportional to the electric field ε,. When the electric field is increase,nonlinearities appear in the mobility and carriers in the channel will have an increased velocity. In high field, charge carriers gain and lose their energy rapidly particularly through phonon emission until the drift velocity reaches a maximum value called velocity saturation. .A plot of electron drift velocity versus electric field is shown in fig(5)



Fig(5) variation of velocity with electric field

The mobility of the carriers reduces at higher electric fields normally encountered in small channel length devices due to velocity saturation effects .At higher field there is no longer a linear relation between the electric field & drift velocity as the velocity gradually saturates reaching the saturation velocity.

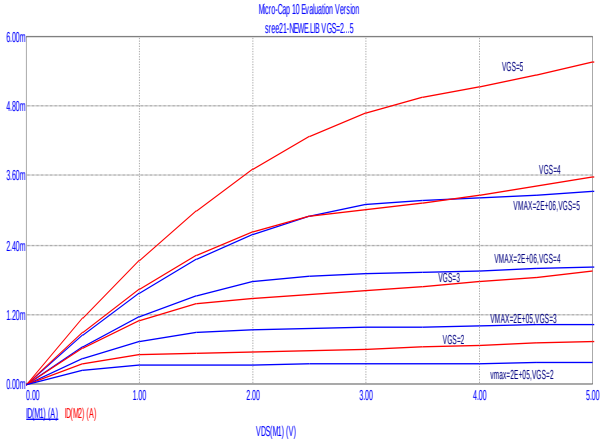
In sub-micron MOSFETs one finds that the average electron velocity is larger than in bulk material so that velocity saturation is not quite as much of a restriction as initially thought.The effect of velocity in longchannel NMOSFET is shown below in fig(6).To investigate the limiting effects of velocity saturation use spice level3 model with maximum drift velocity of $3x10^6$



Fig(6) .The output chara with and without velocity saturation

In long channel at high electric field mobility can be approximated by $\mu_n=V_{sat}/E$. For long channel devices,$V_{s1}>>V_{gt}$ and $V_{dsat} \rightarrow V_{gt}$ as predicted by the constant mobility model, hence, the velocity saturation effects are not too important for long channel devices.Where V_s is the saturation limited thermal velocity. where $V_{gt}=V_g-V_T$. The role of velocity saturation due to high-field mobility degradation in lifting the pinchoff condition in a long-channel MOSFET is described in[6].

However, for modern day MOSFETs, the typical gate length is much smaller than 1µm , velocity saturation effects are extremely important.Fig(6) investigate the effect of velocity saturation on output current in scaled MOSFETs.



Fig(6),Limitation of I_D in scaled device with and without velocity saturation (Vmax=2e+06)

From fig (6)for nMOSFETs with $L < 1$ um, V_{sat} causes current to saturate for $V_D < (V_G - V_{th})$.

$$\therefore I_{DSAT} \cong WC_{ox}(V_G - V_{th})v_{sat} \qquad (14)$$

Thus I_{DSAT} α V_G-V_{th} for short L devices instead of square law.In short channel devices the magnitude of the electric field is comparably higher than long channel devices,where the channel length is comparable to the depletion region width of the drain and source. Here, Secondary Order Effect (SOE) exists . For a long channel device, simulation shows a linear behavior; however, for short channel devices, it shows a significant departure from linearity a measure of whether the device is a short-channel or a long-channel device.Velocity saturation reduces the transconductance in saturation mode.This occurs in shortchannel devices when the dimensions are scaled without lowering the bias voltages. Using *Vde(sat)*, the maximum gain (g_m)possible for a MOSFET can be defined as

$g_m = C_{OX} V_{de(sat)}$ (15)

Charge-based continuous equations for the transconductance and output conductance of Channel submicrometer Graded-(GC) Silicon-On-Insulator (SOI) Nmosfet is proposed by [7]

2.The impact of temperature on drain current in scaled MOSFET device

There are two primary temperature-dependent effects in MOS devices. The first is a change in threshold. The other effect, that of mobility reduction with increasing temperature, tends to ominate because of its exponential nature.The temperature coeiffient of Vth is approximate 1mv/^{0}C for modern CMOS.

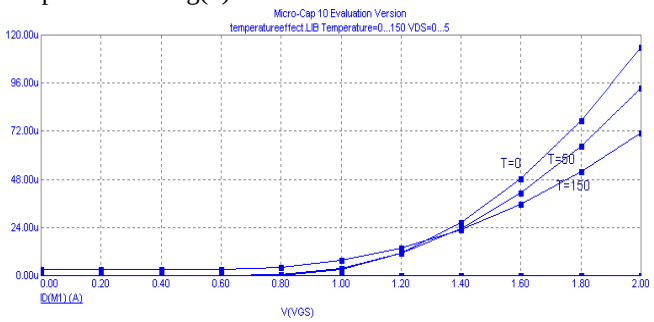
In long channel devices when temperature increases , the mobility decreses .Reduction in mobility causes the I_D to go down as in (16)

$I_{D\,SAT} = \mu.\varepsilon_{ox}/2t_{ox}$ W/L $(V_{GS}-V_{TH})^2$ (16)

Threshlod voltage and mobility can be written as a function of temperature as

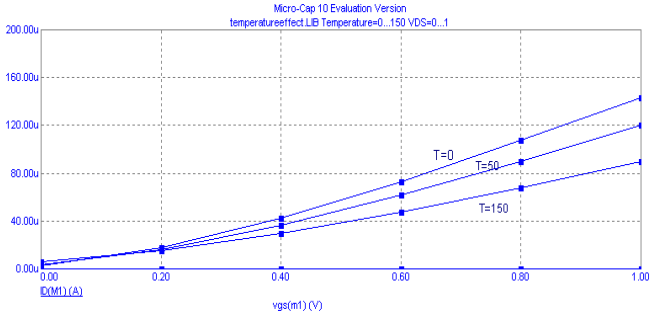
$V_{THN}(T) = V_{THN}(T_0)\,(1+TCV_{THN}(T-T_0)$ (17)

where TCV_{THN} is the temperature coefficient of the threshlod voltage,V_{THN} measured at the temperature T_0. T is the temperature ,T_0 is the room temperature (300K),m is the mobility temperature coefficient . It is seen from [11] and [12] that the mobility andV_{THN} shows negative dependence on temperature. Same time decrease in V_{TH} causes the I_D to increase . This effect is analized by simulation ,in long channel is shown below using level 44 with three different temperature in fig(7)



Fig(7) The effect of temperature on drain current in longchannel devices

A two dimensional temperature dependent analytical model of Gate Stack Insulated Shallow Extension Silicon On Nothing (ISESON) is presented by[8].The[9] propose a universal current-based definition of the threshold voltage (V_T) and discusses some direct methods to measure it. Fig(8) shows how the drain current changes with temperature in a scaled device with channel length =100nm.



Fig(8) The imapct of temperature on output current in short channel

Result shows that at a fixed bias, the drain current decreases as the temperature increases. At low V_{GS} ,the changes in V_{THN} become more significant and it can be cancel out the effect of the change in the mobility and Vsat.When the Vgs is very high ,change in V_{THN} is relatively insignificant compared to the changes in mobility and saturation velocity .As a result the temperature dependence of the drain current follows that both u/Vsat, are negative.In shortchannel devices alternatively, variations in carrier mobility are higher for devices in the 65nm CMOS technology as compared to variations observed in the 180nm CMOS as in [10]. Also it propose new design methodology based on scaling the supply voltage for suppressing the current variations due to temperature fluctuations. Temperature fluctuation induced propagation delay variations in CMOS integrated circuits are examined in the paper. [11]. A new compact temperature-dependent model for the ON-current is presented based on the

alpha-power law and is verified with BSIM3as in [12]. In [13] Device parameters that characterize the variations in MOSFET current due to temperature fluctuations are identified for 180nm and 65nm CMOS technologies.

V.CONCLUSION

The paper, analyzed impact of temperature on the drain current both in long channel and scaled devices . It is observed that at a fixed gate to source voltage , the drain current decreases as the temperature increases.It also examined the limitation imposed on electron drift characteristics in the channel that is becomes more pronounced in short channel devices as they operate at high electric field. It yields smaller drain saturation current and voltage value than that predicted by the ideal long channel relation. It decreases the effective mobility of the transistor . The capability of long channel models is limited as they are unable to provide an accurate representation of drain current model for short channel devices due to a lack of physicals component consideration. The Overall analysis provide a solid basis to conclude that, the temperature and velocity attributes a limitation on drain currents in scaled device .

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