Modelling and Simulation of Dynamic Voltage Restorer for Power Quality Improvement

H.Lakshmi, T. Swapna

Abstract-- The dynamic voltage restorer (DVR) is used to regulate the voltage at the load terminals from various power quality problems like sag, swell, harmonics, unbalance etc., in supply voltage. This paper presents modelling aspects of several types of Dynamic Voltage Restorer (DVR) working against various voltage sags by simulation in PSCAD/EMTDC. The reference signal for the series connected DVR is obtained indirectly from the extracted load terminal reference voltage. It then provides analyses of working performance of the device, including capability and quality of compensation. Significant simulation results show that these several types of the modelled device can work very well against balanced and/or unbalanced voltages caused by faults in a distribution system. In addition, appropriate ways to obtain a good quality output voltage by a DVR during voltage sag is also presented.

Index Terms--Dynamic Voltage Restorer (DVR), voltage sag, balanced and unbalanced faults, power quality, sag severity, harmonic distortion.

I. INTRODUCTION

THE importance of power quality (PQ) has risen very considerably over the last two decades due to a marked increase in the number of equipment which is sensitive to adverse PQ environments, the disturbances introduced by nonlinear loads, and the proliferation of renewable energy sources, among others. At least 50% of all PQ disturbances are of the voltage quality type, where the interest is the study of any deviation of the voltage waveform from its ideal form [1]. The best well-known disturbances are voltage sags and swells, harmonic and interharmonic voltages, and, for three-phase systems, voltage imbalances.

Power quality in the distribution system is widely studied due to its impact on some sensitive loads [1]. Power quality problems include sags, swells, transients and other distortions to the sinusoidal waveform [1]. The new group of devices called custom power devices [2] are developed and installed for the improvement of power quality in the distribution system. They are mainly of three categories such as shunt connected distribution static compensator (DSTATCOM), series connected compensator like dynamic voltage restorer (DVR) and unified power quality conditioner (UPQC) which is connected in both shunt and series. The series connected compensator can regulate the load terminal voltage from the 'low quality' supply voltage and protect the critical consumer loads from tripping and consequent loss. Dynamic voltage restorer (DVR) was originally proposed to compensate for voltage disturbances on distribution systems. A typical DVR scheme is shown in fig.1

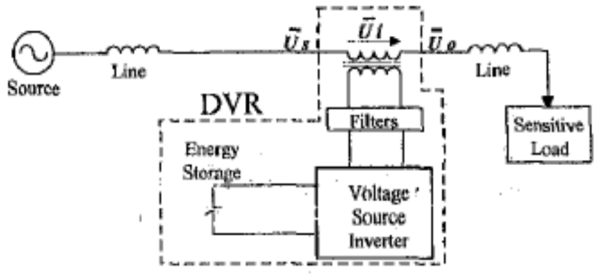

Fig.1. A typical DVR scheme

A voltage sag is normally caused by short-circuit faults in the power network [2], [3] or by the starting up of induction motors of large rating [4]. The ensuing adverse consequences are a reduction in the energy transfers of electric motors and the disconnection of sensitive equipment and industrial processes brought to a standstill. A comprehensive description of voltage sags can be found in [5].

Harmonics are produced by nonlinear equipment, such as electric arc furnaces, variable speed drives, large concentrations of arc discharge lamps, and loads which use power electronics. Harmonic currents generated by a nonlinear device or created as a result of existing harmonic voltages will exacerbate copper and iron losses in electrical equipment. In rotating machinery, they will produce pulsating torques and overheating. Voltage imbalances are normally brought about by unbalanced loads or unbalanced short-circuit faults, thus producing overheating in synchronous machines and, in some extreme cases, leading to load shutdowns and equipment failure. The DVR is essentially a voltage-source converter connected in series with the a network via an interfacing transformer, which was originally conceived to ameliorate voltage sags. However, as shown in this paper, its range of applicability can be extended very considerably when provided with a suitable control scheme. The basic operating principle behind the DVR is the injection

- *H. Lakshmi, received Masters Degree in High Voltage Engineering Power Systems from Ramappa Engineering College, JNTU, India, PH-09989660311, E-mail: lakshminagurla@gmail.com*
- *T. Swapna, received Masters Degree in Digital Systems & Computer Electronics from Vagdevi Engineering College, JNTU, India, PH-09849643369, E-mail: swapnathota@gmail.com*

of an in phase series voltage with the incoming supply to the load, sufficient enough to reestablish the voltage to its presages state.

There are typically four main components to model a DVR:

- Coupling transformer
- DC voltage source
- Multi-pulse bridge inverter
- Control system

The coupling transformer with either a delta or wye connection on the DVR side is installed on the line in front of the protected load. Filters can be installed at the coupling transformer to block high frequency harmonics caused by DC-to-AC conversion to reduce distortion in the output. The DC voltage source is an external source supplying DC voltage to the inverter to convert to AC voltage. The optimization of the DC source can be determined during simulation with various scenarios of control schemes, DVR configurations, performance requirements, and voltage sags experienced at the point DVR is installed. The inverter is a six-pulse gate turn off (GTO) thyristor controlled bridge. Currents will follow in different directions at outputs depending on the control scheme, eventually supplying AC output power to the critical load during power disturbances. The control of this bridge is indeed the control of thyristor firing angles. Time to open and close gates will be determined by the control system. There are several methods for controlling the inverter. To model a DVR protecting a sensitive load against only balanced voltage sags, a simple method of using the measurement of three-phase rms output voltage for controlling signals can be applied. Amplitude modulation (AM) is then used. In addition, to provide appropriate firing angles to thyristor gates the switching control using pulse width modulation (PWM) technique and interpolationfiring is employed.

II. MODEL OF THE DVR-CONNECTION SYSTEM

Atypical test system, incorporating a DVR, is depicted in Fig. 2. Various kinds of loads are connected at the point of common coupling (PCC), including a linear load, a nonlinear load, and a sensitive load. The series connection of the voltage-source converter (VSC) making up the DVR with the ac system is achieved by means of a coupling transformer whose primary is connected in series between the mains and the load. Although a passive LC filter is normally used to obtain a switching-ripple-free DVR voltage, in this paper, this filter is not considered in order to fully assess the harmonic cancelling properties of the repetitive controller.

Fig. 3 shows the equivalent circuit for the DVR, where v_s is the supply voltage, Z_s is the line impedance, i_s is the current supplied by the source, which splits at the PCC into a current injected into the sensitive load *i* and a current injected into other loads i_r. The voltage v_{pcc} is th measured voltage at the PCC, *u* is the voltage representing the DVR, which is modeled as an ideal voltage source.

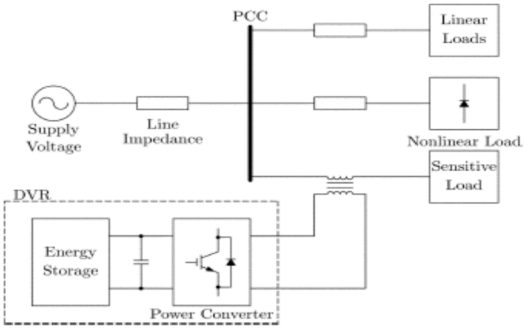

Fig .2. System configuration with a DVR

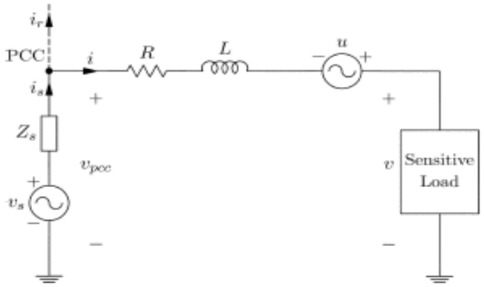

Fig. 3. Single-phase equivalent circuit for the DVR.

Also, *R* and *L* are the resistance and inductance of the coupling transformer, respectively, and *v* is the measured voltage across the sensitive load. The sensitive-load voltage *v* can be obtained as

$$v(t) = v_{pcc}(t) + u(t) - Ri(t) - L\frac{di}{dt} \quad \ldots\ldots (1)$$

Voltage sags in an electrical grid are almost impossible to avoid, because of the finite clearing time of the faults that cause the voltage sags and the propagation of sags from the transmission and distribution system to the low-voltage loads. The theory of voltage sags and interruptions for electrical networks is thoroughly described in [6]. Voltage sags are a common reason for failures in production plants and for end user equipment malfunctions in general. In particular, tripping of equipment in a production line can cause production interruption and significant costs of lost production. One solution to this problem is to make the equipment itself more tolerant to sags, either by intelligent control or by storing “ride-through” energy in the equipment. An alternative solution, instead of modifying each component in a plant to be tolerant against voltage sags, is to install a plant-wide uninterruptible power supply (UPS) system for longer power interruptions or a dynamic voltage restorer (DVR) on the incoming supply to mitigate voltage sags for shorter periods. DVRs can eliminate most sags, and minimize the risk of load tripping for very deep sags, but their main drawbacks are their standby losses, the equipment cost and also the protection scheme required for downstream short circuits.

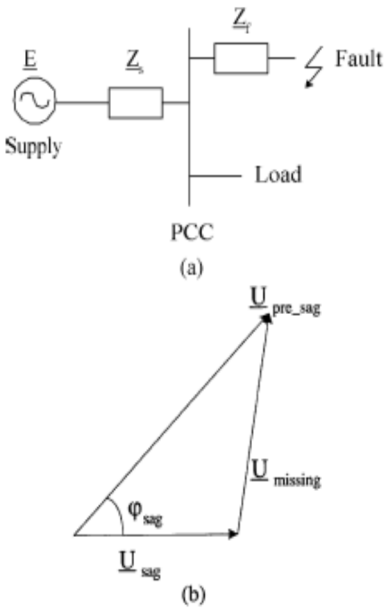

Fig.4. Origins of voltage sags (a) Circuit (b) Vector diagram

Many solutions and problems using DVRs have been published in recent years. Industrial examples of DVRs are given in [7]–[8], while more future problems/possibilities associated with DVRs are discussed in [9]..

Voltage sags are usually caused by a short circuit current flowing into a fault on a transmission or distribution line. This is shown on the simplified grid model of Fig. 4(a), where the magnitude and phase of the faulted voltage $\underline{U}_{sag}$ during the sag at the point of common coupling (PCC) are determined by the supply impedances using the equation

$$\underline{U}_{sag} = \underline{E}\frac{\underline{Z}_f}{\underline{Z}_f + \underline{Z}_g} \quad \text{..... (1)}$$

where

$\underline{u}_{sag}$ Voltage during the sage at PCC;

$\underline{E}$ Supply voltage;

$\underline{Z}_s$ Supply impedance:

$\underline{Z}_f$ Impedance at faulted line.

$\underline{u}_{sag}$ differs from the prefault voltage $\underline{u}_{pre-sag}$ by $\underline{u}_{mis\sin g}$, as shown in phasor form in Fig. 1(b)

Voltage sags can be symmetrical or nonsymmetrical. However, most voltage sags are nonsymmetrical, as identified in a recent Electric Power Research Institute (EPRI) survey. Sags may be generated by: three-phase faults, three-phase faults with ground connection, two-phase faults, two-phase faults with ground connection, and single-phase faults.

III. DVR CONTROL STRATEGY

The proposed control algorithm is derived from the algorithm presented in [10] in which the shunt compensator is controlled for harmonic current compensation, load current balancing and power factor correction. Here, the sag, swell, harmonic voltage and unbalance in supply voltage are compensated by controlling the DVR. The load terminal voltage is regulated and the waveform is controlled to sinusoidal. The proposed control scheme is shown in Fig. 5.

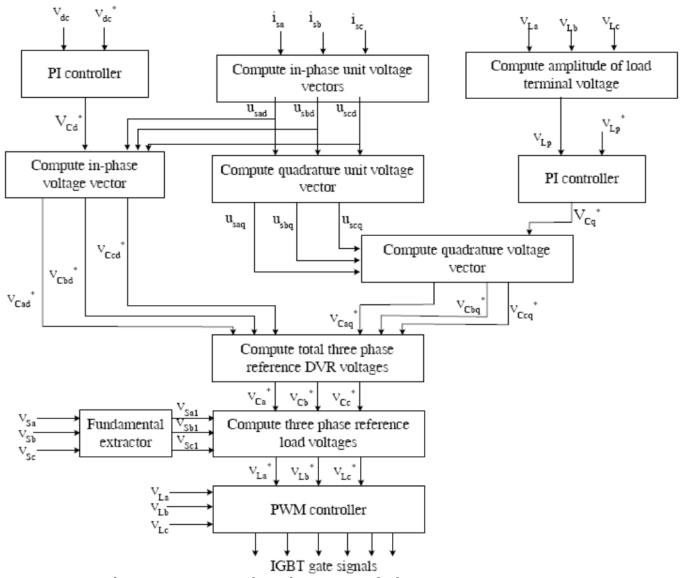

Fig. 5 Control scheme of the DVR

The reference signal for the load terminal voltage (vLa *, vLb *, vLc *) is extracted from the sensed load terminal voltages (vLa, vLb, vLc), supply currents (iSa, iSb, iSc), supply voltages (vSa, vSb, vSc) and the dc bus voltage (vdc) of DVR as feed back signals. There are two proportional-integral (PI) controllers used to estimate the in-phase and quadrature components of the injected fundamental voltage by the DVR. The harmonic voltage to be injected is estimated from the sensed supply voltage (vSa, vSb, vSc) by extracting the fundamental component (vSa1, vSb1, vSc1) of it.

Three phase unit voltage templates (uSad, uSbd, uScd) are derived in-phase with the supply currents (iSa, iSb, iSc). The dc bus voltage of the DVR is regulated using a PI controller over the sensed (vdc) and reference values (vdc *) of dc bus voltages. This PI controller output is considered as the amplitude (VCd *) of the in-phase component of the injection voltages (vCad *, vCbd *, vCcd *) derive the amplitude (VLp *) of the quadrature component of the injection voltages (vCaq *, vCbq *, vCcq *) of the DVR by using it over the amplitude of sensed load voltage (VLp) and reference value (VLp *) of the load terminal voltage. The fundamental component of the supply voltage (vSa1, vSb1, vSc1) is extracted from the sensed supply voltage (vSa, vSb, vSc) using the synchronous reference frame (SRF) transformation. The reverse of the SRF transformation after filtering the dc component gives the fundamental component of the supply voltage. The algebraic sum of the inphase component (vCad *, vCbd *, vCcd *), the quadrature component (vCaq *, vCbq *, vCcq *) and the fundamental of supply voltage (vSa1, vSb1, vSc1) are taken as the reference load voltages (vLa *, vLb *, vLc *). A pulse width modulation (PWM) controller is used over the reference (vLa *, vLb *, vLc *) and sensed load voltages values (vLa, vLb, vLc) to generate gating signals for the IGBT's (insulated gate bipolar transistors) of the VSC. The carrier wave (triangular)

frequency is set at 10kHz. The gating pulses switch the IGBT's of the VSC for the compensation of sag, swell, unbalance and harmonics in supply voltage.

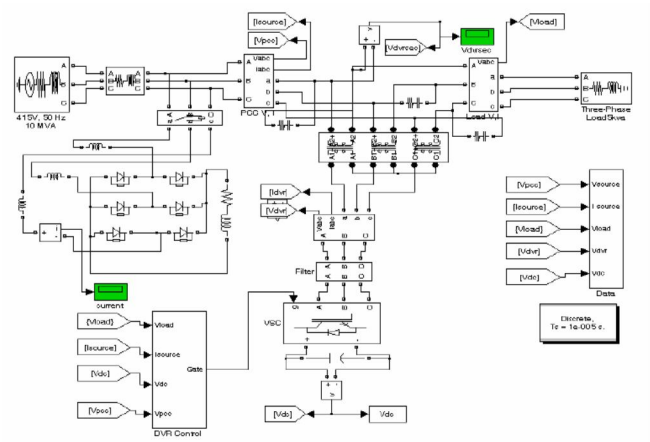

Fig. 6. MATLAB model of the DVR connected system

IV. MATLAB BASED SIMULATION OF DVR SYSTEM

Fig. 6 shows the MATLAB model of the DVR connected system. The supply voltage is realized by using a three-phase voltage source and source impedance is connected in its series. In order to simulate the disturbances at the PCC voltage, an additional load is switched on with a circuit breaker. The load considered is a lagging power factor load. The DVR is connected in series with the supply using an injection transformer. The VSC is connected to the transformer along with a ripple filter. The dc bus capacitor is selected based on the transient energy requirement and the dc bus voltage is selected based on the injection voltage level. The dc capacitor decides the ripple content in the dc voltage. The system data are given in Appendix. The reference load terminal voltages are derived from the sensed supply voltages, supply currents, load terminal voltages and the dc bus voltage of DVR.

V. PERFORMANCE OF DVR SYSTEM

The performances of the DVR for different supply disturbances is tested under various operating conditions. The proposed control algorithm is tested for different power quality events like voltage sag (Fig.7), voltage swell (Fig. 8), unbalance in supply voltage (Fig. 9) and harmonics in supply voltage (Fig.10). Fig. 7 shows a balanced sag of 30% in supply voltage at 0.15 s and occurs for 5 cycles of ac mains. The DVR injects fundamental voltage (vc) in series with the supply voltage (vs). The load terminal voltage (vL) is regulated at the rated value. The supply current *(is*), amplitude of supply voltage (*VSp*) the amplitude of load terminal voltage (*VLp*) and the dc bus voltage (vdc) are also shown in the Fig.7.

The dynamic performance of the DVR for a swell in supply voltage is given in Fig.7. The load voltage (vL) is regulated at rated value, which shows the satisfactory performance of the DVR. The supply current *(is*), the amplitude of load terminal voltage (*VLp*), the amplitude of supply voltage (*VSp*) and the dc bus voltage (vdc) are also shown in the Fig. 7. The dc bus voltage is regulated at the reference value, though small fluctuation occur during transients.

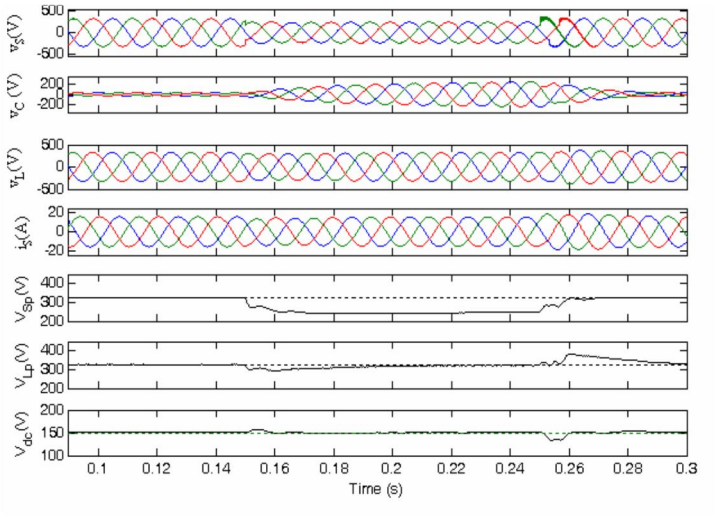

Fig. 7 Compensation of supply voltage sag using DVR

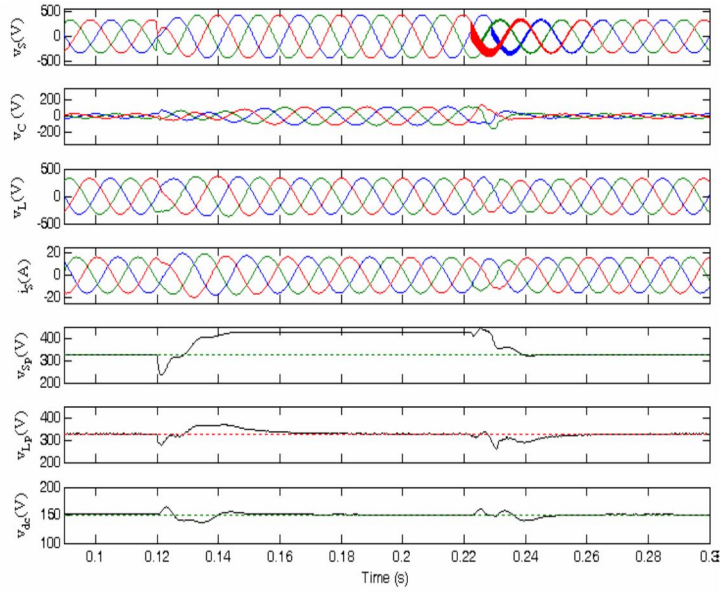

Fig. 8 Compensation of supply voltage swell using DVR

The performance of DVR for an unbalance in supply voltage is shown in Fig. 9. The phase voltages at the PCC are different in magnitude at 0.2s as given in the voltage at PCC (vs) of Fig. 9. Now the DVR injects unequal fundamental voltages (vc) so that the load terminal voltage (vL) is regulated to constant magnitude. The supply current *(is*), the amplitude of load terminal voltage (*VLp*), the amplitude of supply voltage (*VSp*) and the dc bus voltage (vdc) are also shown in the Fig. 8 to demonstrate the satisfactory behavior of DVR.

The harmonics compensation in supply voltage is tested and depicted in Fig. 10. The voltage at PCC is disturbed by switching on of a non-linear load and the load terminal voltage (vL) is undistorted and constant in magnitude due to the injection of harmonic voltage (vc) by the DVR. The load terminal voltage (vL) has a total harmonic distortion (THD) of 1.2% (Fig. 10) at the time of disturbance

and the voltage at PCC has a THD of 7.33% (Fig. 12). The supply current is also sinusoidal with a THD of 0.14%(fig.13).

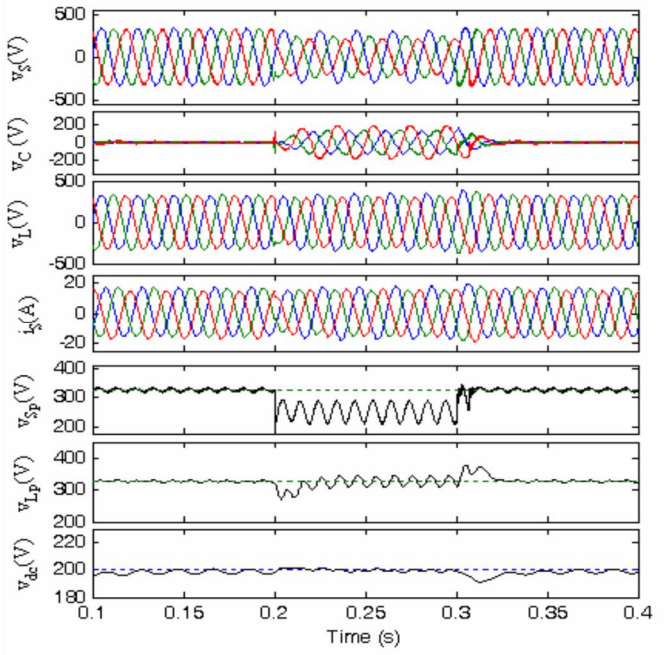

Fig. 9 Compensation of supply voltage unbalance using DVR

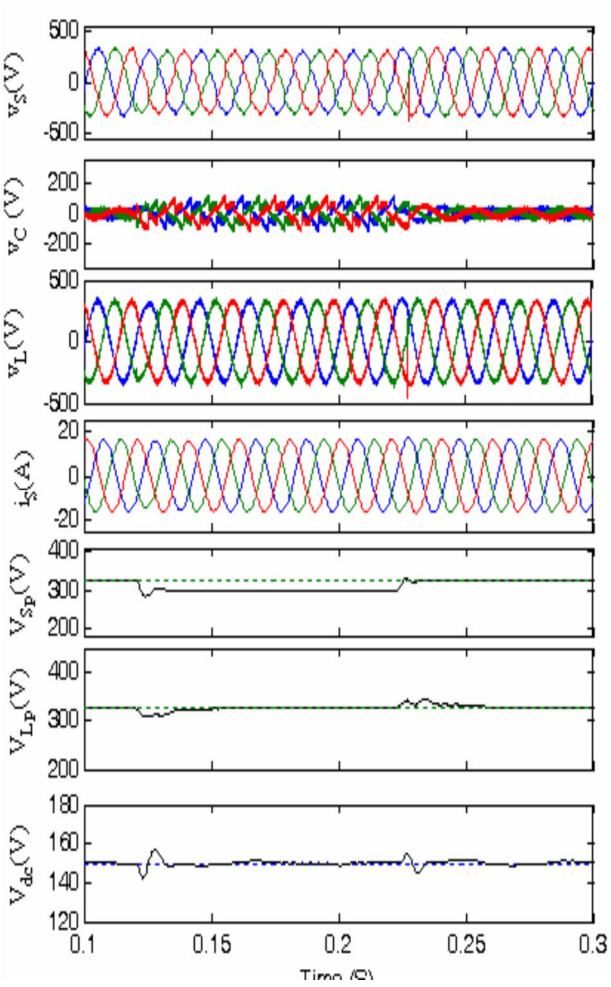

Fig. 10 Compensation of supply voltage harmonics using DVR

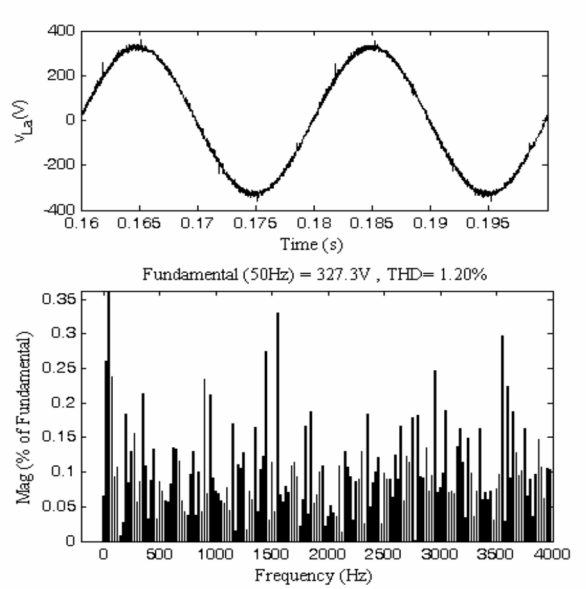

Fig. 11 Load voltage along with harmonic spectrum

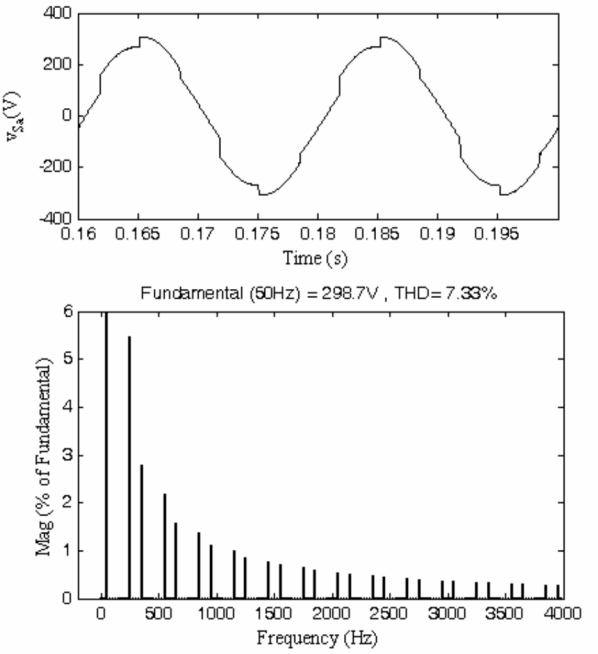

Fig. 12 Voltage at PCC along with harmonic spectrum

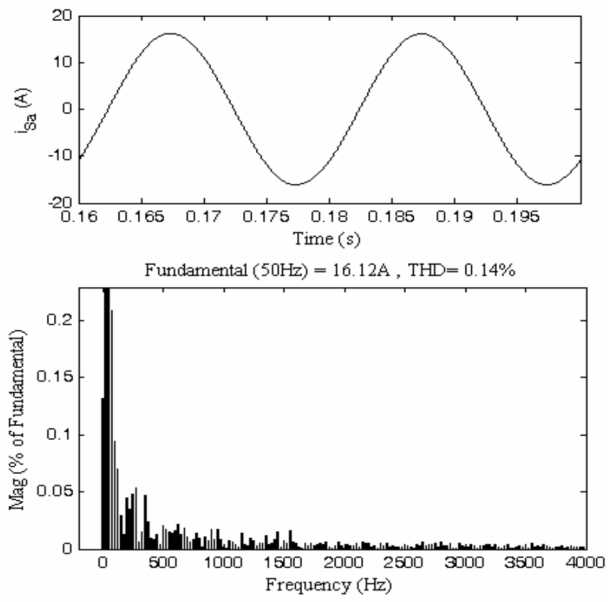

Fig. 13 Supply current along with harmonic spectrum

VI. CONCLUSION

The proposed control scheme of DVR has been validated through computer simulation using MATLAB software along with simulink and power system block set toolboxes. The reference voltages for the DVR has been obtained indirectly by extracting the reference load terminal voltage. The performance of the DVR has been observed to be satisfactory for various power quality disturbances like sag, swell, unbalance and harmonics in supply voltage. Moreover, it is able to provide self-supported dc bus of the DVR through power transfer from ac line at fundamental frequency.

The parameters of the system considered are:
Line Impedance, Ls=3.5mH,Rs=0.01Ω
Load: 8.5kVA, pf : 0.707lag
Ripple filter: r r C =1⌠F,L =□3.1mH
DC bus voltage: Vdc =150V
DC bus capacitance: dc C =1000⌠F
AC line voltage: VLL =415V, 50Hz ,
PWM switching frequency: 10kHz

Transformer: 20kVA,100V / 400V
Transformer: 20kVA,100V / 400V

VI REFERENCES

[1] M. H. J. Bollen, “What is power quality?,” *Elect. Power Syst. Res.*, vol. 66, no. 1, pp. 5–14, July 2003.
[2] J. G. Nielsen and F. Blaabjerg, “A detailed comparison of system topologies for dynamic voltage restorers,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1272–1280, Sep./Oct. 2005.
[3] V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, C. Zhan, M. Barnes, and N. Jenkins, “Supervisory control of dynamic voltage restorers,” *Proc. Inst. Elect. Eng., Gen., Transm. Distrib*, vol. 151, no. 4, pp. 509–516, Jul. 2004.
[4] P. T. Nguyen and T. K. Saha, “Dynamic voltage restorer against balanced and unbalanced voltage sags: Modelling and simulation,” in *Proc. IEEE Power Eng. Soc. General Meeting*, Jun. 2004, vol. 1, pp. 639–644, IEEE.
[5] M. H. J. Bollen*, Understanding Power Quality Problems: Voltage Sags and Interruptions.*. Piscataway, NJ: IEEE Press, 2000.
[6] M. Bollen, *Understanding Power Quality Problems, Voltage Sags and Interruptions*. Piscataway, NJ: IEEE Press, 1999.
[7] T. Jauch, A. Kara, M. Rahmani, and D. Westermann, “Power quality ensured by dynamic voltage correction,” *ABB Rev*, vol. 4, pp. 25–36, 1998.
[8] T. Sezi, “Kompensation von spannungseinbrüchen im mva-lastbereich,” *Etz*, vol. 9, pp. 20–23, 2001.
[9] G. Joos, “Three-phase static series voltage regulator control algorithms for dynamic sag compensation,” in *Proc. ISIS ’99*, vol. 2, 1999, pp. 515–520.
[10] A. Chandra, B. Singh, B.N. Singh and K. AI-Haddad, “An improved control algorithm of shunt active filter for voltage regulation, harmonic elimination, power-factor correction, and balancing of nonlinear loads“, *IEEE Trans. on Power Electronics, v*ol. 15 no. 3, pp 495 – 507, May 2000.

Lakshmi H Received the B.Tech (Hons.) Degree in electrical and electronic engineering from the University of Kakatiya University, Warangal in 2007,and received the Master Degree in Power Systems High Voltage Engineering from Ramappa Engineering College Warangal, JNTU,HYD .