Design of Low power, Low Jitter Ring Oscillator Using 50nm CMOS Technology

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Abstract A modified ring oscillator presented in this paper. The voltage control oscillator is designed and simulated in 50nm CMOS technology. The frequency of oscillation of the VCO is 2.6GHz with 0.064 mW power dissipation and the center drain current of 64uA is used. Tuning range is of 72% and the jitter is of 39.8pS.

Index Terms Voltage Controlled Oscillator (VCO), power dissipation, jitter, tuning range, phase locked loop (PLL)

1 INTRODUCTION

Wireless and Wire line communication systems such as wireless Local Area Network, Mobile and Satellite communication, backplane interconnects and chip-to-chip communication systems, clock generation and skew compensation in microprocessors and other communication devices are widely used Phase Locked Loop(PLL) as a basic building block[3].The VCO jitter performance in these applications can impact the output clock's timing jitter which often limits the system performance [9] .Also in most of the narrow band communication systems the frequency synthesizer plays a major role in generating local oscillation signal or carriers and is usually implemented through a PLL[5].The high power consumption in the frequency synthesizer is mainly due to the VCO therefore one of the most challenging building block of the PLL is the VCO .Among many other oscillator topologies the ring oscillator is attractive for its high frequency ,wide range of operation and small die size. A ring oscillator consists of multiple stages of delay cells. Delay cell can be design with differential pair and CMOS inverter. In this paper CMOS inverter is used as a delay cell [7].

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2 VCO Design

VCO is a frequency modulated oscillator whose instantaneous output frequency is directly proportional to its control voltage .A ring oscillator can be smoothly integrated in a standard CMOS process without taking extra processing steps because it does not require any passive resonant element compare to CMOS LC-tank oscillator [6], [7], [8].In this work 5-stage CMOS inverter forms a closed path with positive feedback [10]. The schematic of the whole VCO is shown in fig 1.Voltage control oscillator have a CMOS inverter circuit as shown in figure2.This inverter circuit is connected to current sources M3 and M4 that limit the current available to the inverter. The currents in MOSFETs M1 and M2 are mirrored in each inverter stage.

2.1 Oscillation frequency

The oscillation frequency is given by –

$$f_{osc} = \frac{I_d}{N C_{tot} \cdot V_{DD}} \quad (1)$$

Where,

N= Number of stages

$I_d = I_{d3} = I_{d4}$ = center drain current

$$C_{tot} = C_{out} + C_{in} \quad (2)$$

$$C_{tot} = C'_{ox}(W_p \cdot L_p + W_n \cdot L_n) \quad (3)$$

$$C_{in} = \frac{3}{2} C'_{ox}(W_p \cdot L_p + W_n \cdot L_n) \quad (4)$$

$$C_{tot} = \frac{5}{2} C'_{ox}(W_p . L_p + W_n . L_n) \quad (5)$$

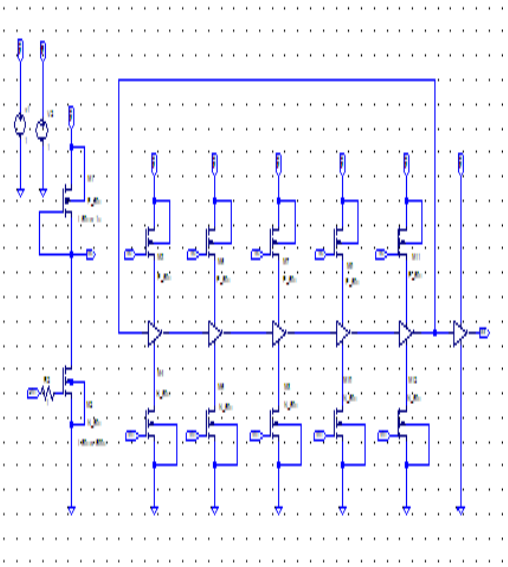

Figure 1 Schematic view of VCO

2.2 Tuning range

VCO designed such that its oscillation frequency is controlled by input voltage. For communication it is important to have a large tuning range among the other structure of VCO ring oscillator has a large tuning range [4].Tuning range is shown in fig 3. Tuning range can be defined as-

$$\text{Tuning range}\% = \frac{f_{max} - f_{min}}{f_{center}} \times 100 \quad (6)$$

Where

$f_{center} = f_{osc} =$ frequency of oscillation

f_{max} = Maximum frequency

f_{min} = Minimum frequency

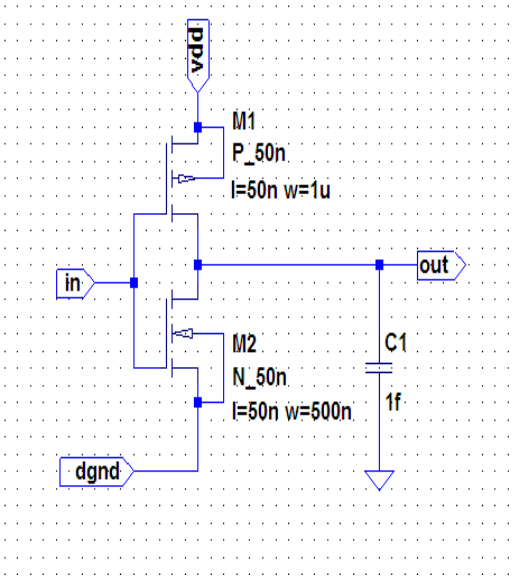

Figure 2 Schematic view of CMOS inverter

2.3 Gain

Gain of the VCO is the slope of the curves given in fig3.It is defined as

$$K_{VCO} = 2\prod\left(\frac{f_{max} - f_{min}}{V_{max} - V_{min}}\right) \text{ radian/v.s} \quad (7)$$

2.4 JITTER

It is the interval between two times of maximum effect (or minimum effect) of a signal property that varies regularly with time. It is defined as-

$$\Delta t_{jitter} = \frac{1}{f_{center}} - \frac{1}{f_{center} + \Delta f_{VCO}} \quad (8)$$

Δf_{VCO} = Variation in the VCO's output frequency.

f_{center} = frequency of oscillation

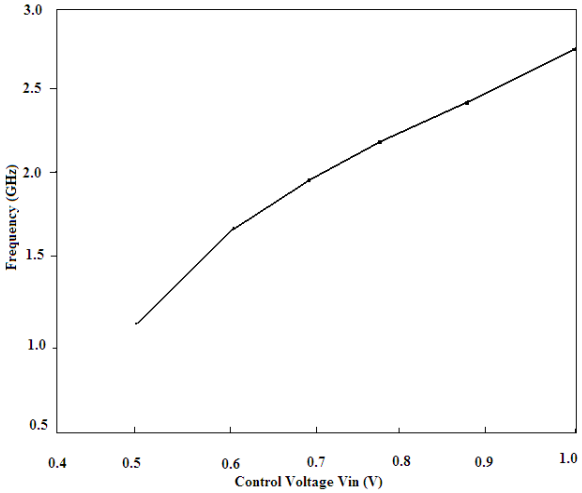

Figure3: graphical representation of frequency vs. voltage

2.5 Power dissipation

The average power dissipated by the VCO is given as [11]-

$$I_{avg} = N.V_{DD}C_{tot}.f_{osc} \quad (9)$$

$$p_{avg} = V_{DD}.I_{avg} \quad (10)$$

$$I_{avg} = I_d \quad (11)$$

$$p_{avg} = V_{DD}.I_d \quad (12)$$

3 EXPERIMENTAL RESULTS

The ring oscillator for this work has been realized in 50nm CMOS technology. The output frequency can vary from 0.7GHz to 2.56GHz, the tuning range is found to be 72%

which is much better than what is reported earlier. At 2.56 GHz the average power consumption is 0.064mW at 1V supply voltage which is also much lesser compared to 65nm and 180nm designs. The jitter for the circuit is 39.8pS. The performance result of the Voltage control oscillator compared with earlier work is summarized in Table 1.

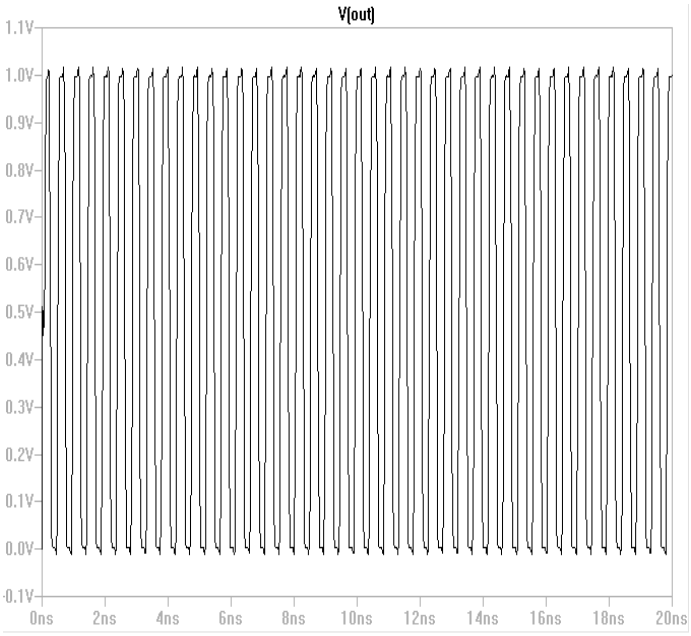

Figure 4 Simulation result of output voltage vs. time

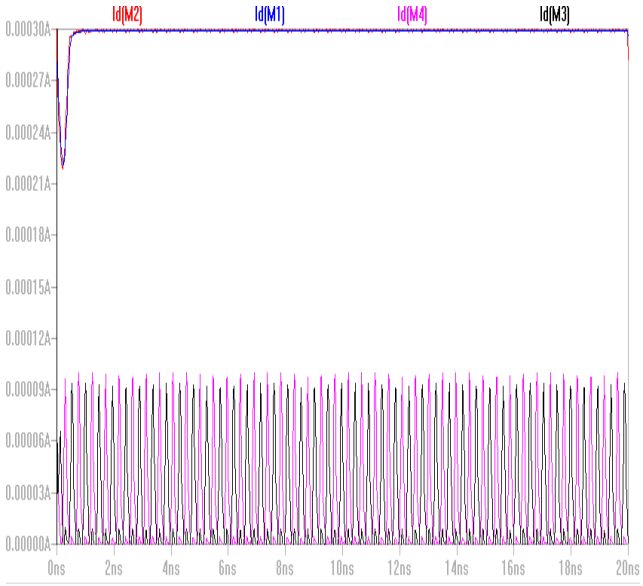

Figure 5 Simulation result of drain current

Table1. Comparison with state of art

Work	[2]	[1]	This work
Max. frequency(Hz)	5.89G	800M	2.56G
LC/Ring	LC	Ring	Ring
Frequency range(Hz)	4.65-5.89G	2-40M	0.7-2.56G
Operating voltage	1.3V	1.8V	1V
Technology	65nm	0.18um	50nm
Power consumption	4.8mW	3mW	0.064mW
Tuning range	-	24%	72%
No. of stages	-	1	5
Jitter	-	-	39.8pS

4 CONCLUSION

The design presented in a 50nm CMOS technology and is designed using CMOS inverter with current mirror .The Voltage control oscillator consumes power around 0.064mW for 1V supply and the tuning range is 72%.

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