CMOS BASED THERMAL ENERGY GENERATOR FOR LOW POWER DEVICES

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Abstract— This paper presents a thermal energy generator (TEG) designed using complementary metal oxide semiconductor (CMOS) process which converts thermal energy into electrical power. Energy harvesting techniques provide viable option to improve battery performance of low power devices. TEGs are of special interest due to its energy efficient, have no moving part and free maintenance. Secondly, thermal energy or heat gradient is an unremitting energy that is abundantly found from various sources such as the sun, industrial machines, automotives, mobile systems and human body. The proposed energy harvesting device takes advantage of the temperature differences between the hot to cold parts to produce an electrical power and provides a solution for micro-scale electronic systems. A 220 pair of thermopiles made of *n*-doped and *p*-doped polysilicon materials are electrically connected in series and thermally connected in parallel. Simulation shows that at a temperature gradient of 3 K, the proposed device can produce an output voltage and power of 0.29 V and 0.04 mW, respectively. Compatibility of the proposed TEG design with the standard CMOS processes enables to realize a novel on-chip power supply capable of powering many low-power wireless sensor networks and devices.

Index Terms— CMOS based TEG, Thermal energy harvesting, Polysilicon, Seebeck effect, Thermocouple, Thermoelectric generator.

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1 Introduction

RENDs in current electronic technologies are reduction in **L** terms of device sizes but increasing the performances. Wireless sensor networks (WSNs) have been utilized in various applications ranging from structural monitoring for buildings and bridges, homeland security, aircraft engine monitoring, agriculture to biomedical applications [1-3]. Furthermore, over the past several years, low power electronic technology has become more imperative [4] and are widely used in consumer applications such as smartphones, hearing aid and cardiac pacemaker. Batteries have so far been employed as the power source for the devices. However, batteries exhibit several disadvantages. The use of batteries limit the lifetime of these devices. Power can only be provided over finite period of time [5] due to power drain. Replacement and recharging of batteries will significantly increase the cost and lead to serious environmental pollution [6]. Thus, other possibilities need to be lookout to reduce dependency on batteries. A promising solution to this problem is to use energy harvesting technologies. Energy is found in the target environment of these devices in several forms such as kinetic, thermal and radiation energy. The process of extracting these energies into electrical energy is known as energy harvesting, or energy scavenging. Negligible maintenance effort [7] is require and unlimited power source can be provided using energy harvesting technique.

There are two types of energy harvesters which are macro and micro types. Macro-energy harvesters mainly focus to reduce carbon emission and for oil dependency. The sun, wind, tides and waves are the most suitable energy sources for the macro- energy harvesters. Typical power produced by macro-energy harvester ranges from kilowatts to megawatts. For micro-energy harvester, the ultimate goal is to power up wireless sensor networks and wearable devices [8]. Among the energy harvesting technologies, TEG is of special interest as a micro-energy harvester. TEGs are prevailing, as they are robust, environmental friendly, have no moving part, compact and provide virtually limitless lifetimes [9]. Abundant waste heat available in the ambience can be converted into electrical

energy by using Seebeck effect. With the recent rapid advancement, the CMOS technology has become the predominant fabrication technology. With the aid of CMOS technology, extreme miniaturization of various sensors and actuators has been achieved [10,11]. Furthermore, capabilities of monolithic circuit integration are enhance through CMOS process. Thus, realizing a micro-scale TEG device has becomes a significant research subject in order to scavenge thermal energy that is suitable for low-power applications and wearable devices.

In this paper, the design, modeling and simulation of a micro-scale TEG, compatible with the CMOS fabrication technology is presented. The *p*-doped and *n*-doped polysilicon is chosen as the material of the TEG thermopile, as it is available and can be monolithically integrated in the normal CMOS manufacturing line. The proposed design is simulated to foresee the temperature distribution in the structural parts of the TEG. The temperature difference predicted in the simulation step is used to obtain the output voltage and power.

2 THEORY OF TEG

The term thermoelectric is literally associated with thermal and electrical phenomena. TEG is a solid state device that can convert thermal energy from a temperature gradient into electrical energy [12]. Typically, there are three main thermoelectric effects which are Seebeck effect, Peltier effect and Thomson effect [13].

Seebeck power generation or Seebeck effect is a phenomenon by which an electromotive force or a potential difference is produced by a circuit made of two wires of dissimilar materials when the junctions of the two wires are maintained at different temperatures. This phenomenon was discovered by T. J. Seebeck in 1821. In 1834, 13 years after Seebeck made his discovery, Jean Peltier discovered the reverse process of Seebeck effect –the Peltier effect. He discovered that the passage of an electric current through a thermocouple produces heating and cooling effects depending on the direction of the current. The relation between Seebeck effect and Peltier effect was later on discovered by W. Thomson in 1855 and is known as

Thomson effect. This law relates to the rate of generation of reversible heat which results from the passage of a current along a portion of a single conductor along which there is a temperature difference [14].

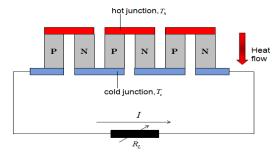


Fig. 1. Schematic of TEG.

A simple electrical circuit of a TEG is shown in Fig. 1. TEG device consists of an array of thermoelectric couple (thermocouple) composed of two elements: p-type and n-type semiconductors that are connected thermally in parallel and electrically in series to form a thermoelectric module. Heat is transferred from the hot temperature junction, T_h at the rate of

 Q_h to the cold temperature junction, T_c at the rate of Q_c . To simplify the theoretical analysis, it is assumed that the contact resistance is neglected and all the thermoelectric elements have the same length, L and area, A. Seebeck coefficient, thermal conductivity and electrical resistivity are assumed to be temperature independent. Furthermore, it also assumed that heat transfer only happens due to conduction by thermoelectric elements. The assumptions made above are reasonable when the temperature difference between the two junctions is small. Heat generations in a TEG are resulted from the Joule heating, heat associated with the Seebeck effect and thermal conduction. The heat flow at the hot junction can be described as

$$Q_{h} = \alpha_{pn} T_{h} I - \frac{1}{2} I^{2} R + K (T_{h} - T_{c})$$
(1)

In a similar way, we can obtain the heat balance equation at the junction at temperature, T_{c} as

$$Q_{c} = \alpha_{pn} T_{h} I + \frac{1}{2} I^{2} R + K(T_{h} - T_{c})$$
 (2)

where I is the current and K is thermal conductance. As heat flows from the hot to the cold junction, free charge carriers (electrons from n-type and holes from p-type) are also driven to the cold end. Thus, when an electron conducting (n-type) leg and hole conducting (p-type) leg are connected, an output voltage is produced.

Output voltage related to Seebeck effect is best described with correlation in Eq. (1)

$$V = \alpha_{pn} \Delta T \tag{3}$$

where $\alpha_{\scriptscriptstyle pn}$ is the relative Seebeck coefficients of the p-type

and n-type semiconductor elements and ΔT is the temperature gradient between the hot junction, T_h and the cold junction, T_c . Output voltage is proportional to the temperature gradient and the relative Seebeck coefficients. Seebeck coefficient of a material is also known as thermopower. It is a measure of the magnitude of an induced thermoelectric voltage in response to a temperature difference across the two junctions and it is dependent on the molecular structures of the materials and the absolute temperature .

The Seebeck coefficient of *p*-type and *n*-type semiconductor elements can be obtained from Eq. (4) and Eq. (5) given below

$$\alpha_p = \frac{k_B}{q} \left\lceil \frac{5}{2} - \left\lceil \left(\frac{E_i - E_f}{k_B T} \right) \right\rceil \right\rceil \tag{4}$$

$$\alpha_n = -\frac{k_B}{q} \left[\frac{5}{2} - \left[\left(\frac{E_f - E_i}{k_B T} \right) \right] \right] \tag{5}$$

where α_p and α_n are the Seebeck coefficient of the p-type and the n-type semiconductor respectively, k_B is the Boltzmann constant, q is the elementary charge, E_i and E_F is the intrinsic Fermi energy and Fermi energy of the materials used and T is the temperature of dopants.

The performance or the efficiency of a TEG is governed by the properties of the thermoelectric material which is represented by the figure of merit (Z). The figure of merit of a material is given as

$$Z = \frac{\alpha^2}{\rho k} \tag{6}$$

where α is the Seebeck coefficient , ρ is the electrical resistivity and k is the thermal conductivity. To achieve an adequate value of Z, a high Seebeck coefficient with low electrical resistivity and low thermal conductivity are indispensable.

If we considered, the output power is obtained under matched load resistance, the maximum output power can be expressed as

$$P_{\text{max}} = \frac{V^2}{4R} \tag{7}$$

where R is the internal resistance of the TEG. Substituting Eq. (3) into Eq. (7), the maximum power can be expressed as

$$P_{\text{max}} = \frac{\left(\alpha_{pn}\Delta T\right)^2}{4R} \tag{8}$$

If we considered, n- number of thermocouples are connected thermally in parallel and electrically in series, Eq. (6) can be written as

$$P_{\text{max}} = \frac{n^2 \left(\alpha_{pn} \Delta T\right)^2}{4R} \tag{9}$$

3 LITERATURE REVIEW

Many studies have employed Seebeck effect to generate electricity from heat gradient. For a macro-scale TEG, Ahmad Nazri *et al.* [15] have designed an energy harvesting device based on Seebeck effect. The dimension of this device is 40 mm x 40 mm x 3.2 mm with a relative Seebeck coefficent of of 42.36 mV/K and an internal electrical resistance of 0.03 Ω . The device is capable to produce 5.5 V to 6 V output voltage at ΔT = 80 °F and the output current is measured at 400 to 500 mA. Bavel *et al.* [16] fabricated EEG system using thermoelectric fundamental in headband with a total hot plate area of 64 cm². It was designed in ten sections of 1.6 x 4 cm² each. The TEG produced 2 to 2.5 mW of power. Hongyun *et al.* [17] developed a hybrid power source consisted of solar cells and TEG. Results showed that the open circuit voltage was 0.3 V for a device with dimension of 150 mm x 80 mm x 24 mm.

Micro-scale TEGs have also been reported in literature. Ziyang Wang et al. [18] fabricated a TEG chip consisted of 4700 thermocouples by using micromachining technology. The authors were able to produce 0.25 V open circuit output voltage for a 1 K of temperature difference. Open circuit output voltage per unit temperature difference per unit area was measured at 12.5 VK-1cm-2 and the output power was measured at 0.026 µWK-2cm-2. Till Huesgen et al. [19] fabricated a TEG device by using combined surface and bulk micromachining processes. An output voltage of 9.51 mVK-1 was obtained from this device under a temperature gradient of 1 K. Kockmann et al, [20] presented a 1 cm² microstructured TEG with 7500 thermocouples. Wang et al. [21] modeled a thermoelectric micro generator based on p-type and n-type Bismuth Telluride (Bi₂Te₃) material by using MEMS technology and achieved a Seebeck coefficient of about 260 and -188 µV/K.

Commercially used materials for TEG is Bi₂Te₃. Bi₂Te₃ is a promising semiconductor compound, as it provides high thermoelectric figure of merit (FOM). However, it is less compatible with the standard micromachining techniques and extra efforts are needed to make it compatible with CMOS processes. Thus, it is vital to find the best material, companionable with normal CMOS process line. It may be noted that a low thermal conductivity, large Seebeck coefficients and low electrical resistivity make a material an excellent choice for a TEG device. Doped polysilicon has been utilized as thermoelectric material in many reported research works. Polysilicon is able to solve the compatibility issue and possesses the aforementioned characteristics of a suitable material for a TEG.

Several works related to CMOS TEG based polysilicon materials have been reported. Jin Xie $\it et~\it al.$ [22] presented the design, modeling, fabrication and characterization of a TEG. Materials used by the authors are phosphorus and boron heavily doped polysilicon thin films. The device area was 1 cm² . At a temperature gradient of 5 K, an open circuit voltage of 16.7 V and an output power of 1.3 μW , under matched load resistance, were reported. Hsu Kao $\it et~\it al.$ [23] presented a thermoelectric micro generator fabricated by using 0.35 μm CMOS process. Experimental results showed an output voltage of 67 μV at a temperature gradient of 1 K. Yang $\it et~\it al.$ developed a TEG using standard CMOS process [24]. This device was able to produce a power factor of 0.0427 $\mu W/cm^2$ K² and voltage factor of 3.417 V/cm² K.

4 DESIGN OF CMOS BASED TEG

Fig. 2 illustrates the schematic of CMOS TEG design. The harvester consists of 220 thermocouples in series. Phosphorus and boron doped polysilicon is utilized to create *p*-type and *n*-type semiconductor elements. Thermocouple is arranged on the top of the substrate. One junction of the *p*-type and the *n*-type polysilicon legs is coupled to the hot part of the TEG, and the other junction of the *p*-type and the *n*-type polysilicon legs is connected to the cold part. Materials used for the hot plate is made from aluminium. Aluminium is utilized to act as heat receiving area to conduct heat from the hot part to the cold part of TEG. In order to increase the temperature difference between the hot and the cold junctions, heat must flow through the thermopile from the hot to the cold junction. To achieve this, the hot part is isolated from the cold part by using trenches.

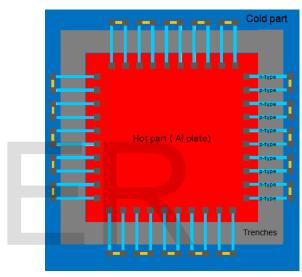


Fig. 2. CMOS TEG design.

The working principle of the proposed device is based on Seebeck effect. All the thermocouples are electrically connected in series in order to obtain an array of thermocouple elements.

TEG is designed to meet the requirements given in Table 1. These requirements are decided based on the previous research works and current technology that is available and suitable for CMOS harvesters.

Table 1. Requirements for CMOS TEG

Temperature gradient (ΔT)	3 K
Open Circuit Voltage (V _{open})	> 0.5 V
Load Resistance (R _{load})	< 1000 Ω
Output Power (P)	~1 mW
Current (I)	~ 1 mA

To meet the given requirements, the optimized values of the design parameters are given in Table 2. The theoretical model presented in section 2 is used to optimize the parameters of the TEG design.

Table 1. Structure parameter

Properties	l (µm)	w (μm)	t (µm)
•		• /	• •

Substrate	3000	1300	100
Thin Film	3000	1300	5
Thermocouple	300	10	0.5
Hot plate	2000	500	1

5 RESULTS AND DISCUSSIONS

CoventorWare, finite element analysis software is engaged to simulate the temperature difference between the hot and cold plates of the TEG. First, a 3D model in accordance with the design presented in Fig. 2 is constructed. The device consists of a thick silicon layer followed by a polysilicon layer, oxide layers and metal layers. Metal layers are connected with the polysilicon layer by using vias. The via is made of tungsten. Boundary conditions are defined by setting a temperature of 303 K for the hot plate, 301 K for the cold part, and 300 K for the substrate.

Fig. 3 shows the simulated temperature distribution for the CMOS TEG.

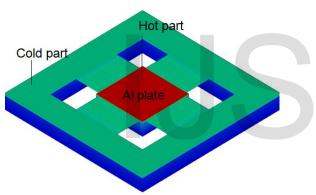


Fig. 1. Temperature distribution of CMOS TEG.

The result showed that for the hot and cold parts, temperature is uniformly distributed. Trenches has successfully isolated the hot part from the cold part. This thermal isolation of the two parts is required in order to achieve a high temperature differences them. Fig. 4 shows the cross sectional temperature distribution in the CMOS TEG

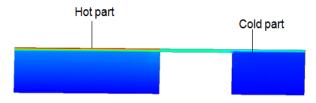


Fig. 2. Cross sectional temperature distribution of CMOS TEG.

Probing is done at the hot part, and temperature is measured at 303 K. At the top surface of the cold part, temperature was set at 301 K and at the bottom part it was set at 300 K. Therefore, when probing was done at the polysilicon layer, temperature was measured at 300 K. It showed a temperature drop of 1 K from 301 K to 300 K across from the top of cold part to polysilicon layer. As the hot plate is heated at 303 K, we can conclude that temperature difference between the hot

junction and cold junction is 3K.

After done with the thermal analysis of the CMOS TEG, output voltage and output power can be calculated using the theoretical model presented in section 2 and prediction of the behavior and performance of the TEG can be made. On the basis of these predictions, the device can be further be optimized for enhancement performance before transferring the layout in 2D for fabrication process. The simulation and formulation results attained are tabulated in Table 3.

Table 3 Simulated performance of CMOS TEG based on simulation and formulation analysis.

Parameters	Value
Seebeck coefficient of p-type, α_p	132 μV/K
Seebeck coefficient of n-type, α_n	-299 μV/K
Relative Seebeck coefficients, $ \alpha_{\scriptscriptstyle pn} $	431 μV/K
Load resistance, R	500 Ω
Open Circuit Voltage, (Vopen)	0.2845 V
Output Power, P_{max}	0.04 mW
Output current, I	0.140 mA

Fig. 5 shows the output voltage versus temperature difference. It is shown that at a temperature gradient of 3 K, this device can deliver an output voltage of 0.2845 V. Graph of the output power versus temperature difference is given in Fig. 6. The output power is measured at 0.04 mW and the output current through a matched load resistance is predicted at 0.140 mA.

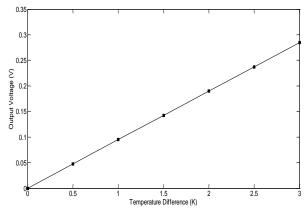


Fig. 3. Simulated result of the output voltage for CMOS TEG.

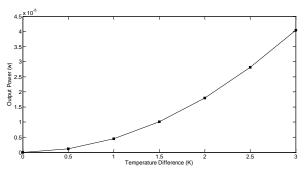


Fig. 4. Simulated result of the output power for CMOS TEG.

6 CONCLUSIONS

A thermal energy generator using CMOS technology has been presented. The proposed CMOS TEG device consists of 220 thermocouples connected in series. Materials used for the thermocouple is *p*-type and *n*-type polysilicon. Doped polysilicon gives high Seebeck coefficient and more importantly, it is more compatible with CMOS process as compared to Bismuth Telluride. The TEG can be extended into an array in order to achieve higher power. An output voltage of 0.2845 V and output power of 0.04 mW is achieved based on the simulation and analytical analysis, proving the feasibility of the concept. Voltage is proportional to the Seebeck coefficients and the temperature gradient between the two junctions of the TEG. Therefore, the performance of the CMOS TEG can be improved if higher temperature gradient can be obtained. Further investigation on the effect of contact resistance is indeed a good way to evaluate the real behavior of the TEG performance. Optimization can also be done towards improving the performance for even larger and complex designs of the TEG.

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